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Short Circuit Power Reduction in Schmitt-Trigger Based SRAM Cell Design

[1]Madhavi.Sowpati, [2]G.Mangarao

[1]Research Scholar, VLSI & ES, Malinenilakshmaiah Engineering College, India

s.madhavi1123@gmail.com

[2]Assistant Professor, E.C.E Department, Malinenilakshmaiah Engineering College, India

mangarao.gunji@gmail.com

Abstract

In low power SRAM Memory cell design power dissipation through standby leakage and dynamic loss is a major problem. This paper is mainly based on low power cell operation and delay of SRAM designing. The paper presents a novel technique to reduce short circuit power. The differential SRAM for ultra low voltage design for Schmitt- Trigger (ST) is analyzed using 180nm cmos technology. Schmitt- Trigger (ST) based differential SRAM cell design helps to sort the issues related to design problems in read and write operation of basic SRAM cell. Feedback is built-in mechanism in proposed Schmitt-Trigger SRAM design. There is always a trade-off among area, power and delay in any SRAM cell designing. In comparison to standard 6T SRAM cell the ST SRAM cell provides better read stability and having a high probability of read failure. Short Circuit power dissipation is one of the considerable parameter in achieving low power. This paper mainly proposes a novel technique for achieving the low power consumption. Delay of an SRAM cell is maintained as it was without affecting the delay with the reduction of power. The read power and write power consumption of an SRAM cell is shown in the following table. By using novel power technique to reduce the short circuit power compared to the proposed design in the paper is reduced by an amount of 21%. The write delay is maintaining constantly even after using the technique to reduce the short circuit power. The performance analysis of the novel design is better than proposed design.

Keywords: Static Random Access Memory, Short Circuit Power, Schmitt-Trigger, Ultra-Low Voltage, Built-In Feedback Mechanism, Stability analysis.

Introduction

Static Random Access Memory (SRAM) provide indispensable on-chip data storage and these are the most dominant component in terms of area, power and delay. In the present generation everything is computerized and there is a necessity to organize and process bulk information which needs to be processed at the instance. In order to cope up with these issues, there needs a efficient memory system, especially in the field of VLSI design. These necessities make memories into limelight of research. While considering on memories there are various types, according to the need. It is a known fact that 4T-SRAM cells have dominated the stand alone SRAM market because of less area overhead. Hence for high density applications a load less CMOS four-transistor (4T) cell for high density embedded SRAM applications [1]. Here power which is one of the important parameter can't be considered for optimization. The minimization of power consumption leads to the improvisation of the battery life time, using various power reduction techniques [1]. The switching power creates a major impact on the total power dissipation, as the supply voltage which is a squaring term in the equation given below

$$P_{dyn} = KfC_{eff}V_{dd}^2 \quad (1)$$

where K is the switching activity factor, C_{eff} is the effective capacitance, and f is the switching frequency. Due to quadratic term in (1), dynamic power may be significantly reduced by scaling down the supply voltage . As the supply voltage is reduced the sensitivity of circuit parameters and process variation increases. Due to the variation limits the SRAM circuit operation are employed with minimum

Corresponding author: Madhavi.Sowpati

sized transistors [2], [3]. The minimal geometrical sizing of transistors leads to the inter-die and intra-die process variation. These type of variations result in a threshold voltage mismatch between the adjacent transistors in a memory cell, thereby asymmetrical characteristics is established [4]. As with higher process variations and lower supply voltage leads to the increase in memory failure such as hold failure read and write failure, and access-time failure, that is the failure on embedded cache memories are due to the scaling the supply voltage.
For any process, the supply voltage V_{dd} at which the transistor operates is determined by the gate oxide thickness. Any change in the voltage V_{dd} depends on the thickness of the gate oxide layer. By scaling the gate oxide thickness reduces the supply voltage V_{dd}.
The rest of this paper is organized as follows. Section II describes on various types of SRAM cells. Section III describes different SRAM cell topologies. Section IV gives the power report of various SRAM cells. Section V uses a technique to reduce the short circuit power. Section VII gives the simulation results of the work. Section VIII shows the power comparison tables. Section IX concludes the work with the comparison report of short circuit power. We use tsmc-180nm CMOS bulk process for all simulations in this paper. We have used H-SPICE to perform all the simulations in this paper.

Static Random Access Memory

Static random-access memory (**SRAM** or **static RAM**) is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The term *static* differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is powered off. SRAM is more expensive and less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.

The SRAM is the major component only occupying larger area of the chip die and for SOC designs, the selection of technology and system designing are mainly depends on digital circuit requirements. There is a high need of demand for Static Random Access Memories (SRAM) in the modern SOC's. SRAM consumes more than 70% of System-On-Chip (SOC). For cache memories, main frame computers and hand-held memory devices SRAM is the significant component.

The power consumption of SRAM varies widely depending on how frequently it is accessed; it **can** be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have nearly negligible power consumption when sitting idle – in the region of a few micro-watts. Several techniques have been proposed to manage power consumption of SRAM-based memory structures. They are general-purpose product and integrated on chip.

SRAM Bit-cell Topologies

Bit density, area, timing specification and low voltage operations are the parameters on which an SRAM bit cells have been proposed. The following figure Fig. 1 lists the SRAM bit-cells having four to ten transistors. A four transistor (4T) load less bit-cell is the one where the PMOS acts as an access transistor [1]. This 4T cell uses two nMOSFETs as a drive transistor and two pMOSFETs to transfer the data in the cell. The advantage of going for load less 4T SRAM cell is that if uses a pMOSFET instead of load elements. This pMOSFET achieves a high node level rises to V_{DD} during read and write operation of the cell. By incorporating the pMOSFET as a transfer transistor instead of load elements helps in achieving a low silicon area and less delay. If the threshold value is adjusted between 0.2 to 0.4V, this 4T SRAM cell operates with high stability.

There are SRAM cells which are asymmetric in nature. One such cell is 5T SRAM. This consists of asymmetric cross coupled inverters having a single bit-line [5]. The voltage across separated bit line is used for both the read and write operations. The pre-charge voltage in the intermediate read bit-line requires dc to ac converter. Across PVT corners to track the read pre-charge voltage would require additional design margins in bit-cell sizing.

The 6T SRAM memory forms the basis for most static random-access memories in CMOS technology. It uses six transistors to store and access one bit. The four transistors in the center form two cross coupled

inverters. In actual devices these transistors are made as small as possible to save chip-area and are very weak. In 6T SRAM bit-cell two nMOSFETs are used as transfer transistors. Single ended 6T SRAM bit cell uses a full transmission gate at one side. This single ended SRAM cell sacrifices write stability for read stability [6].

The 7T asymmetric SRAM cell is used for achieving the less power consumption by cutting off the feedback connection between the two cross coupled inverters. An extra NMOS transistor is used for separating the connection between the inverter pairs before write. This paper also demonstrates the cell transistor sizing to maintain the read/write delay and static noise margin. It reduces the number of times to charge and discharge the large bit lines capacitance to reduce the write power consumption. The chosen transistor sizes for achieving the less power consumption increase the cell area by 17.5% [7] . There are many ways of designing a 7T SRAM bit cell. In single ended 7T SRAM bit cell the write operation needs either an asymmetrical inverter characteristics or uses differential VSS and VDD bias. In another 7T structure extra transistor is added in the pull down path. This sort of designing the cell gives read-disturb-free operation. During the write mode the feedback will be cutoff in the inverter path [7].
Differential 8T SRAM bit cell uses RWL/WWL to perform read and write operation on to the cell. By using the 8T SRAM cell structure we can see much improvement in gains over 6T cell structure. By extra addition of two FET's this incurs an area penality of about 30% [8].

The asymmetric 9T SRAM also provides read-disturb-free operation [9]. This uses a separate read port to decouple the read and write operation which is same as seen in the single –ended 8T bit cell. Here the bit line leakage is reduced by using the stacked read access transistors in the design.

To achieve read-disturb-free operation in the differential 10T bit cell two separate ports are needed to perform read and write independently. The write-ability of bit cell needs write-assist circuits for successful write operation because of series connected access transistors degrades the write ability [10].

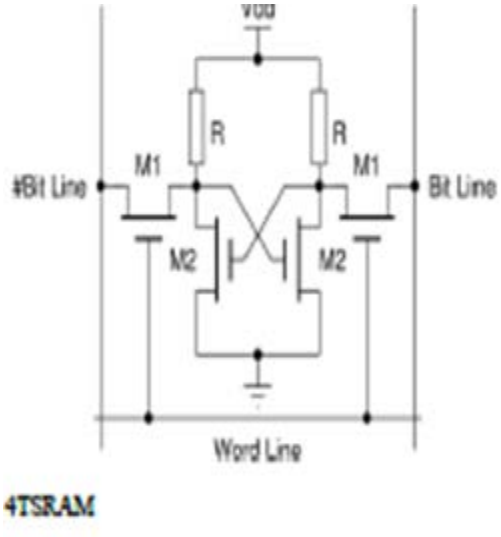

Figure 1:

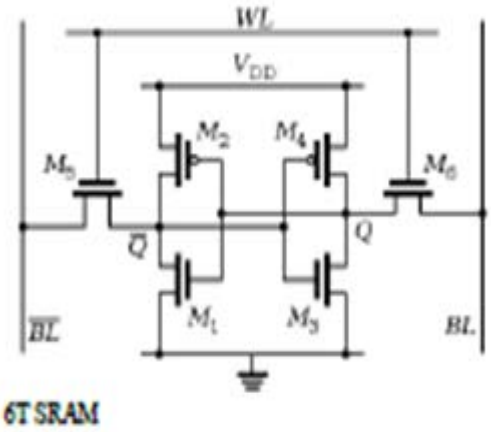

Figure 2:

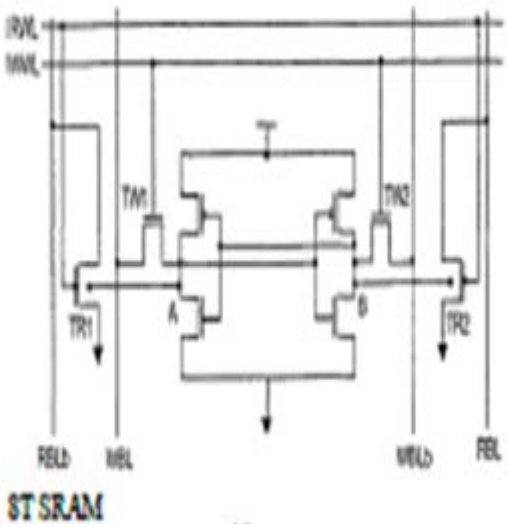

Figure 3:

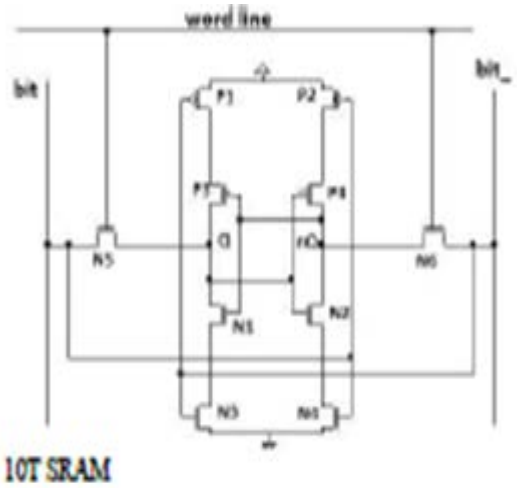

Figure 4: SRAM bit cell Topologies

SCHMITT TRIGGER (ST) BASED SRAM BITCELLS

In the conventional 6T SRAM cell there are conflicts between read and write requirements of design. To resolve these issues in the conventional 6T SRAM cell design we use a Schmitt Trigger principle for the inverter pair in the design. Schmitt Trigger (ST) is used mainly to modulate the switching threshold. In the proposed ST SRAM cell the feedback mechanism is applied only in the pull down path.. By raising the source voltage of NMOS (N1) in pull down path helps to preserve logic "1" using the feedback transistor (NF).

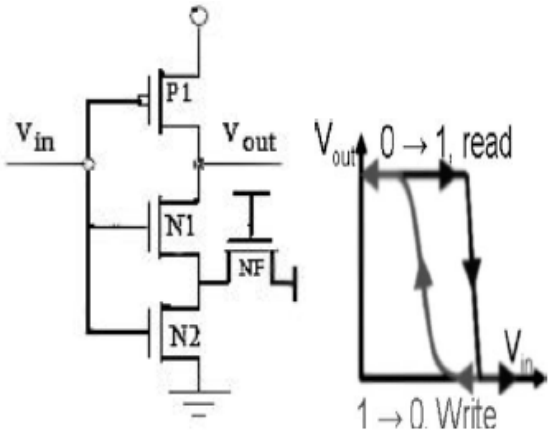

Figure 5: ST schematics

Schmitt trigger helps to achieve robust read operation. This results in smooth transfer characteristics that are essential for easy write operation. In the SRAM bit-cell, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-stability.

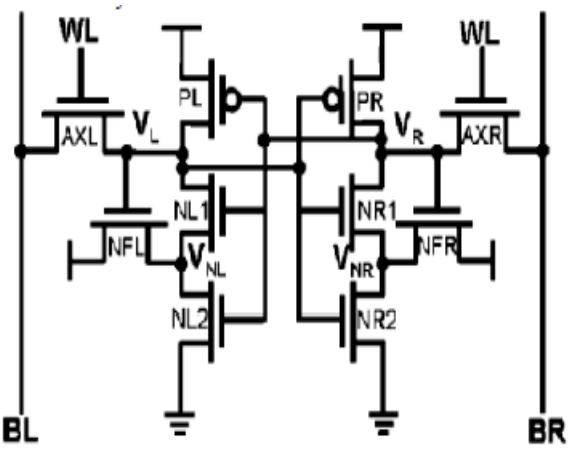

Figure 6: ST1 Bit-cell Schematics

The schematic of ST-1 bit cell is gien in the figure 3. This ST-1 uses ten transistors to perform the required operation. It has one word-line (WL), and two bit lines (BL/BR). There is possibility of forming two ST inverters in the cell. One is PL-NL1-NL2-NFL and the other forms as PR-NR1-NR2-NFR. Two feedback transistors in the pull down path called NFL and NFR used to raise the switching threshold of the inverter during low to high transistion.

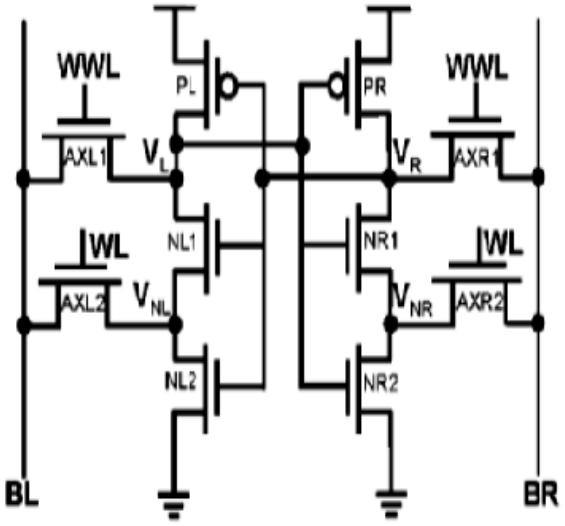

Figure 7: ST-2 Bit-cell Schematics

The ST-2 SRAM cell schematic is shown in the figure 4. There are two word-lines (WL/WWL) and has two nit-line (BL/BR). To operate the cell in the hold mode both WL and WWL are off. Unlike the ST-1 bit cell feedback is provided by separate control signal. The disadvantage in the ST-1 bit cell is the feedback

mechanism is lost during the state transition. In order to improve the feedback mechanism in the ST-1 bit cell, the ST-2 bit cell comes with separate control signal WL to have strong feedback.

Proposed Schmitt-trigger design for short circuit power reduction

The proposed technique in the Schmitt Trigger design helps in achieving the low power and with no change in the delay parameter. The modified SRAM cell technique is compared to the conventional SRAM and we will find the reduction in the parameter power for low power applications. In the proposed technique there is an addition transistors at the two ends of cell. The idea given in this technique breaks the short circuit path in the cell. In this technique, a PMOS is inserted between the VDD and the cell and make sure that it always maintain its gate voltage low. NMOS is inserted between the cell and the ground and applies high at the gate of NMOS[11].

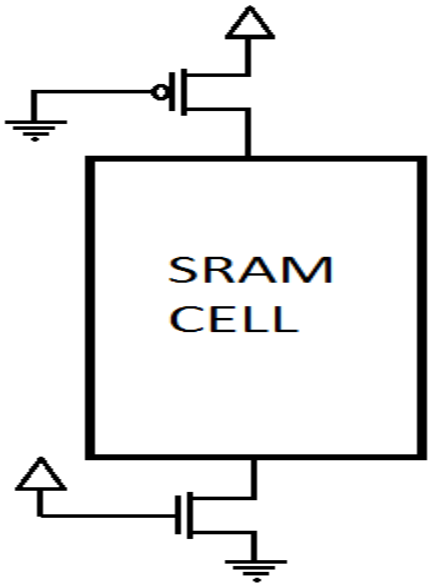

Figure 8: Proposed technique to reduce the power consumption

Proposed technique of ST-1 and ST-2 structures

The proposed technique with ST-1 and ST-2 SRAM cells is shown the following figures. Figure 6 shows the proposed structure of ST-1 SRAM cell and Figure 7 shows the proposed ST-2 SRAM cell.

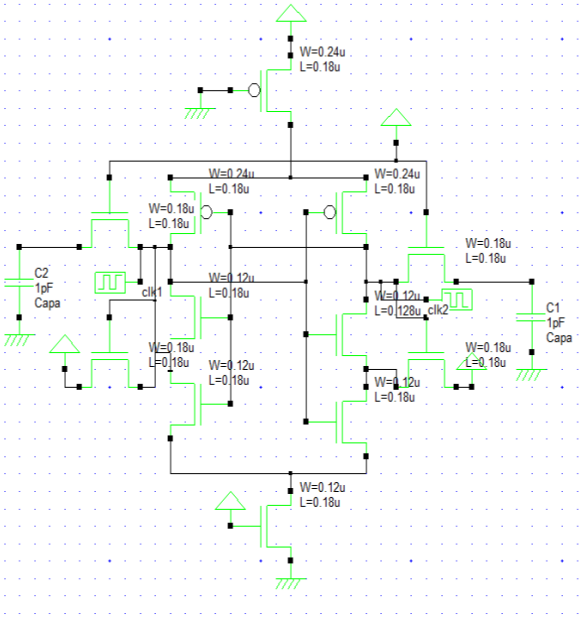

Figure 9: Proposed ST-1 SRAM cell

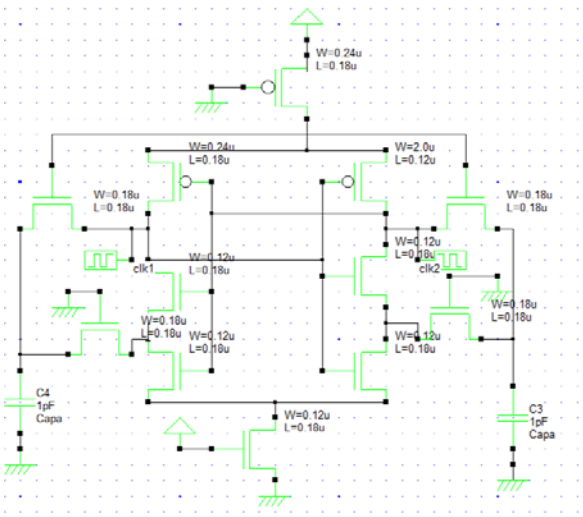

Figure 10: Proposed ST-2 SRAM cell

Simulation Results

The proposed and conventional ST-1 and ST-2 SRAM cells are simulated and the measurements are done . Figure 8 shows the simulation results for conentional ST-1 and ST-2 .Figure 9 shows the proposed simulation results for ST-1 and ST-2 . In the simulation results shown the horizontal axis species timing and the verticla axis represents the voltage. Improements are seen in power consumption with out affecting the delay.

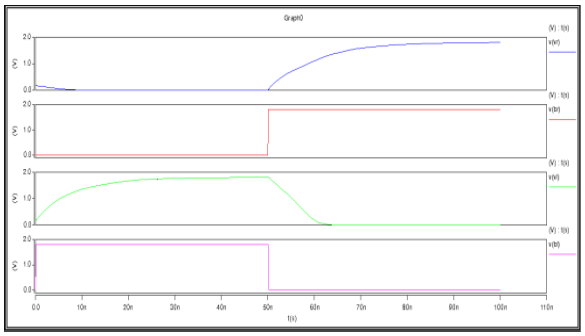

Figure 11: Timing report of ST-1 SRAM cell

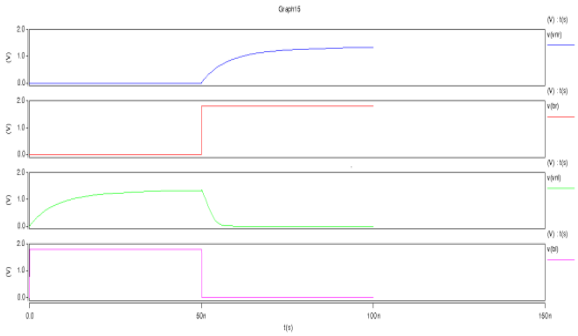

Figure 12: Timing report of proposed ST-1 SRAM cell

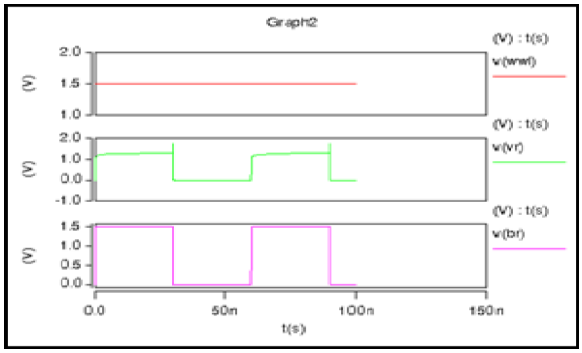

Figure 13: Timing report of ST-2 SRAM cell

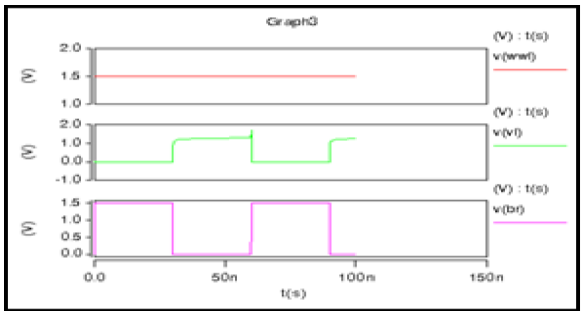

Figure 14: Timing report of proposed ST-2 SRAM cell

Power Analysis

The proposed SRAM cell is designed purely to reduce the Static power flowing in static path dissipation. By adding one PMOS and one NMOS one at the top of the SRAM cell and the other one at the bottom of the cell reduce the static path dissipation.

The following table gives the power report of all conventional SRAM cell structures.

Table 1: Characteristic comparison of various SRAM cell structures in terms of power

S.No	SRAM Architecture	Write Power	Read Power
1	SRAM-4T	7.8936E-04	3.2795E-03
2	SRAM-6T	1.2007E-04	4.5756E-05
3	SRAM-8T	5.7621E-05	4.0190E-05
4	SRAM-10T	1.1163E-04	4.0190E-05
5	SRAM-ST1	1.3705E-04	6.6603E-05
6	SRAM-ST2	3.9589E-05	3.0426E-07

Table 2: Characteristic comparison of various proposed SRAM structures.

S.No	Modified SRAM Architecture	Write Power	Read Power
1	SRAM-4T	2.9511E-04	1.7292E-03
2	SRAM-6T	6.5213E-05	4.5279E-05
3	SRAM-8T	5.5481E-05	4.1217E-05
4	SRAM-10T	5.1972E-07	8.1305E-05
5	SRAM-ST1	9.6079E-05	2.5647E-05
6	SRAM-ST2	3.5620E-05	2.5685E-05

Conclusion

The proposed Schmitt Trigger (ST) based SRAM cell design discussed in the paper mainly helps in reducing the power dissipation during the write operation. This cell reduces short circuit power

flowing from V_{dd} to V_{ss} thus helps in reducing the total power consumed in the cell. Delay of the proposed SRAM cell is maintained as it does not varies the delay with reduction in power. The read and write powers are shown in the tables. This proposed design reduces the short circuit power by an amount of 21% as compared to the conventional design.

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