

Improve performance of johnson counter by reduce number of transistors of d flip flop

Yogesh Sharma¹, Rakesh Jain²

¹M.Tech Scholar, Gyan Vihar University, Jaipur, Rajasthan, India

² Assistant Professor, Dept. of Electronic and Communication, Gyan Vihar University, Jaipur, Rajasthan, India

Abstract

The working of a system is determined by the impact of designing techniques that are implemented over several regions of system. In order to give a smart design & intelligence to design to the computer, a particularized design is requires that can work on low amount of power & has got less complexity. As the computer is comprised of sequential circuitries, there is a need for detecting sequential circuitries in an effective manner & making sure the minimal dissipation of power without any kind of errors & simple architecture. Various counters are taken into account for being cardinal portions of sequential circuitries. In the previous document, a designing schema is considered for developing the Johnson counter along with the required gating of clock that is constituted over toggling operations of J-K FFs. The designing schema is very easy & important than the design based over traditional shift registers as the provided schema furnish lessen interlinks & less dissipation of power. In this paper, we work to enhance the outcome by reduction the amount of transistors of D flip flops. Here, we apply the suggested D-FF in Johnson counter. After the implementation of D-FFs, aggregated amount of transistors will lead to deduction of Johnson counter & area as well.

Keywords: clock gating; Johnson Counter; low power VLSI design; power dissipation; sequential circuit

I. INTRODUCTION

The wing counter is the counter containing circular shift register. The provided are said as hamming distances of two counters that are termed as Johnson & Over beck.

Over beck counter = 2

Johnson counter = 1

There are two forms of ring counters:

Ring counters are having two fluctuations. Those are;

- Over beck counter
- Johnson counter
- Over beck counter

This counter is also defined as straight ring counter. Here, the outcomes of last shift register are combined with the input of first shift. Only one (may be zero) is rotated by the side of ring.

EX: A 4-register one-hot counter which is comprised of initial register values of 1000. We have to identify the repeating pattern.

1000, 0100, 0010, 0001, 1000...

It is to be noted that for the proper functioning, one register needed to be pre-loaded with either 0 or 1.

- Johnson counter

The counter can also e termed as ring counter,

Amoebas counter & Mobius counter. It links the extreme end of outcome of last shift register with the input of initial register & a flow of (value 1s & 0s) is rotated by the side of ring.

EX: A 4-register counter, which is comprised of commencing register values of 0000, we have to identify the repeating pattern.

0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000...

Associatively, it is possible to count the Johnson counters. It work this way as the counters has capability to start over even from the 0s.

A. Johnson Counter (4-Bits)

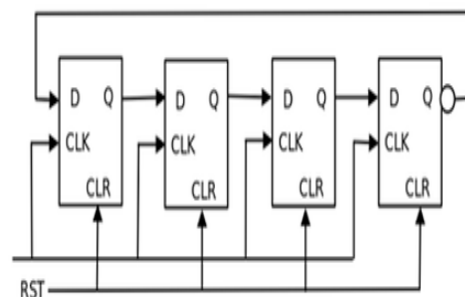


Figure 1: Johnson Counter (4-bits)

It is to be noted that it is possible to create a Johnson counter through inversion of Q signal from previous shift register before an input is fed to initial D flip flop.

How it works

- Green RESET switch is pressed to enable the FFs. [This RESET switch has the working as an on/off switch].
- The outcomes of the FFs are needed to be observed after pressing Red CLK switch. [CLK switch is like a doorbell switch that is generally in off state].
- The D-FF clock is comprised of a rising edge CLK input.

As an illustration, as per behavior of Q

- Q_0 – It is considered as input value D before the CLK rising edge.
- As the CLK rising edge is present, Q_1 is allotted to the last observed D value (Q_0).
- The MOD or amount of unique states of this 3 flip flop Johnson counter is 6.

1.3 JOHNSON RING COUNTER

It can also be referred as 'Twisted Ring Counters' that is a different shift register having the similar feedback as of a basic ring counter. The main difference observed is in terms of the time this inverted outcome Q_0 of previous FF is linked to D input of the initial FF.

1.4 4-BIT JOHNSON RING COUNTER

This surpasses the blocks of four logic '0' & further four logic '1'. Over the end an 8-bit is obtained for a 4-bit Johnson Ring counter as mentioned.

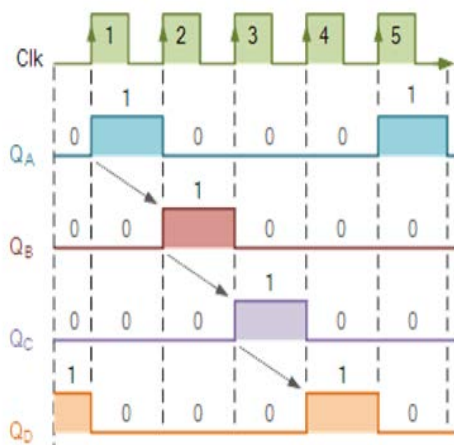


Figure 2: Bit Johnson ring counter

Table 1: Bit Johnson Ring Counter

Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Johnson counter is considered to be useful counter system in the field of computer designing as it possess a precise data pattern in a loop as a synchronous manner that is highly required in various logical designs. In the practical designing, there is a requirement of providing such specified patterns of information to the designated segments of a particular system for establishment of required logical function. For implementing several logics, all types of counter systems can be proven to be effective as each of them gives a different sequence in synchronous forms. All of the operations are executed in synchronous manner that flows up a cycle of clock. Hence, sequential circuitries are highly used in computer designing. Sequential circuitry along the combinational circuitry is incorporated over a chip of smaller area. As the size of chip is reducing, some reliability has become a matter of concern for designers. One of them for CMOS designers is power dissipation. A sequential circuitry system is constituted over clock pulses that lead to dissipation of power in CMOS circuitry. This will be discussed further in more detail.

Several methodologies are applied for minimizing the power dissipation. One of the effective techniques is clock gating. The system of clock gating has numerous advantages like eliminating non-requires clock pulses & implementing effective clock sequences. Various experiments are performed for enhancing the system by making use of clock gating techniques. While it also leads to dissipation of power. Researchers acclaims that 15%-45% of power dissipation is because of clock signals [1]. Hence, by efficient clock management aggregated power dissipation can be reduced to a great extent.

B. Power Dissipation In Sequential Circuits

The logic gates based over CMOS technology are highly efficient in terms of power as almost zero

dissipation of power takes place when they are kept ideal. Dissipation of power was not a matter of concern in the earlier times for various chips. But with furtherance, it has become a crucial issue as with the enhancement in frequency of clock & size of chip [2]. Various forms of dissipation of power are static & dynamic dissipation of power are studied & explained along the way for minimizing them.

Dissipation of power in static form is because of several incidents, in sub threshold conduction like CMOS through the transistors that are not in the active state, oxide gate tunneling current, reverse biased diodes leakage, contention current etc. Dissipation of power in the dynamic form occurs because of discharging of load capacitance & short circuit current while it is in switching state [2]. Various researches are made on the dissipation of power in sequential circuitries for ensuring maximum saving of power [3]-[5]. Sequential logic circuitries are taken into account for contribution to dissipation of power as they are completely regulated by clock input [6]. The clock input tends to make variations in sequential circuitries from their current state in a synchronous manner as per the logic. The sequential circuitries work over only positive or negative edge transitions or on some instances, it can work over both of the edge transitions [7]-[10]. So a sequential circuitry is made operational as per the implemented logic of clock pulses. But on the same instance, a vital combination is given by clock transition that leads to dissipation of power.

Clock transition refers to changes in the value of clock from 0-1 or 1-0. Dissipation of dynamic power in the sequential circuitries leads to transition because of short circuitry in the VDD & ground and also charging & discharging of load capacitance. For explaining the dissipation of power in the clock pulses, a basic CMOS logical inverter is incorporated that is taken as necessary equipment in CMOS architecture.

As a positive edge is given by clock, NMOS will be triggered while PMOS gets deactivated that leads to outcome as 0. As a negative edge is given out by clock, PMOS will be triggered that gives out 1 or VDD over the node producing outcome.

Not going in the same manner of the switching actions, another switching method is provided that contributes to the dissipation of power. In the design of CMOS, both of the PMOS & NMOS are been activated for some instance while the clock transition takes place. The time of rise & fall of clock edges is

ideally taken as 0. But in practical observance, clock is having a particular time of fall & rise (figure 4.2) that cannot be neglected while considering the dissipation of power. On a certain point of fall & rise, both of the PMOS & NMOS are in active state. This produces an electrical path in VDD & ground for passing of current. This current is termed as short circuit current or 'through current'. This current can be observed as spike (figure 3.3) in each clock transition for a small time span.

Passing of current also leads to power dissipation. The consumption of power in transient manner is also caused due to switching current that is needed for charging the internal node in the process of switching. Load capacitances have a major role in CMOS power dissipation.

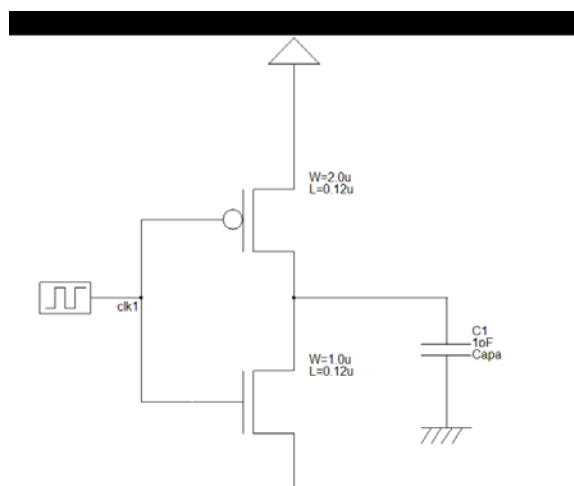


Figure 3: CMOS inverter

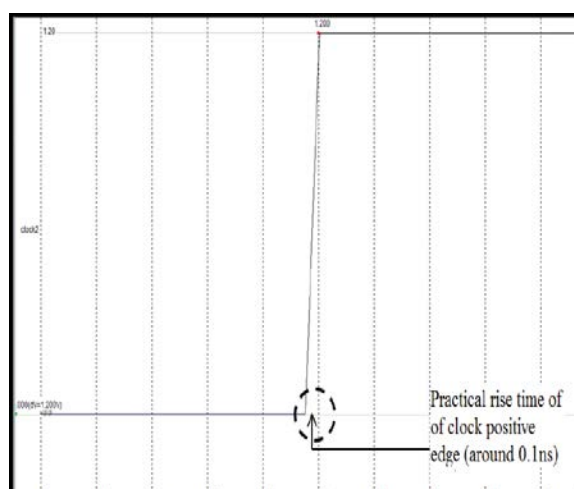


Figure 4: Clock edge rise time

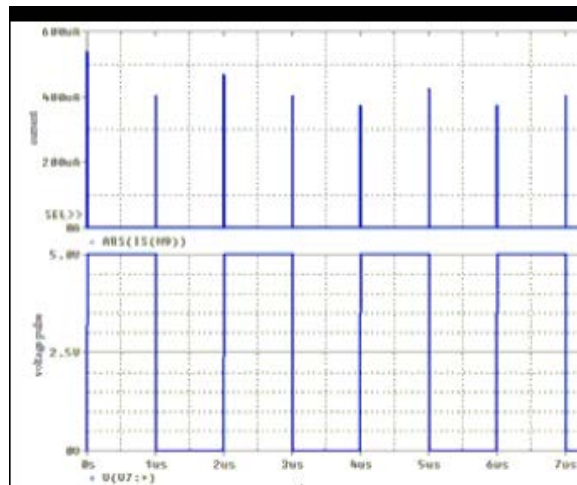


Figure 5: Current spike in Inverter MOSFET due to clock transitions

Half cycle, as PMOS is in active state, load capacitance charges. In the other half cycle, PMOS is deactivated & NMOS is activated, discharging of load capacitance will take place by giving current to ground through NMOS. Thus, in a complete cycle, some dissipation of power takes place because of current given to load capacitance [2].

The concern of dissipation of power matter a lot here because of frequent clock transitions are needed by sequential circuitries for functioning as per applied logic. It is observed that, all of the major types of dissipations are implemented over clock transitions. So there is a high requirement for designing a clock managing or clock gating system that is efficient in regulating the clock pulses over a provided segment of sequential circuitry. On some instances, there is no effect of clock pulse on the values accumulated in the FF as per logic. Such transitions are referred to be as ineffective clock pulse. The values accumulated by the FFs don't get changed logically by these ineffective clock pulses, but it leads to dissipation of power as it leads to switching in the adjoining FFs.

The masking can be done over the clock pulses at a particular instance in a low power design so the clock pulses can go to only that portion of sequential circuitry as it leads to transformation in the values accumulated by it. This method seems to be very efficient for minimizing the dissipation of power [10]-[11].

The suggested Johnson counter is been developed keeping a focus over issues related to dissipation of power. initially, a J-K toggle operation constituted over Johnson counter is designed as fewer interlinks are needed by it that the traditional D or J-K shift

register based over Johnson counter. Additionally, an efficient clock gating system is produced in order of providing clock pulses to FFs as they comes to effect for adjoining FFs, while blocking all of the non-effective modes. The suggested system will be having a major role in reducing the power decadenence of the complete system.

C. Conventional Design of Johnson Counter

Basically a Johnson counter is designed by using a J-K or D-FF constituted over the method of shift registers. The truth table for a 2-bit positive edge counter [12] is provided in Table 4.1. The diagram for a 2-bit Johnson counter is presented in diagram 3.4.

Table 2: Truth table of 2 bit Johnson Counter

State	Q1	Q0	Clock Pulse
S1	0	0	1
S2	1	0	2
S3	1	1	3
S4	0	1	4

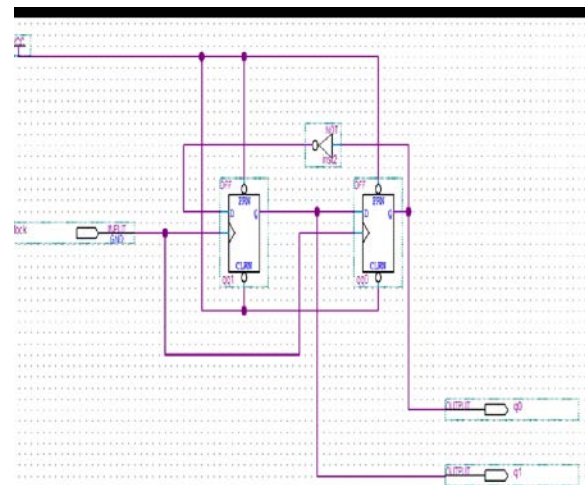


Figure6: Johnson counter (conventional design with D flip-flop)

As the truth table & schema, it is observed that inverted outcome of initial D-FF is linked to D-input of the last D-FF. All the over FFs are provided with the associated D input from the outcome of succeeding FF. a same clock is applied to all of the FFs so that it becomes a synchronous counter system. An N-bit Johnson counter is developed for this suggested design. In this case a single lock is applied to al of the FFs & D-input of any FF will serve as outcome for succeeding FF. while some drawbacks are also observed that are explained below:

D. Absence of Clock Management or Clock Gating System

This system is of synchronous type in which all of the FFs are given the similar clock. As explained in the section II, some unnecessary dissipation of power is produced by non-effective clock pulses in the sequential circuitries. This is the reason that a regulated clock management or clock gating system is required for providing required clock pulses to the linked FFs. As the switching in clock transition takes place, the FF is termed to be in holding state if the current value accumulated by FF is same to the one in earlier state. It means that value of FF is not depending on the switching edge in this mode where the clock pluses that are effective are permitted. The non-effective clock pulses can be blocked at the instance for some FF. this process ensures less dissipation of power [3]-[5]. The figure 5 demonstrates the holding state of 2-bit Johnson counter. The effective clock edges are presented by circling the region for allocated signals of FFs.

E. Interconnections

The interconnections in the constituents are also a manner of concern. In the VLSI design of CMOS, a huge quantity of circuitry constituents is integrated over small space over chip while interconnections are very carefully made. An interconnection may lead to several parasitic & random capacitances. So an effective schema is required for development of routing system that gives fewer issues related to capacitance. It is also observed that the suggested system has more efficiency even after taking the problem of interconnections into consideration. In The previous document [13] for the suggested system is comprised of various clocks that furnish individual services.

F. Master Clock

Master clock is referred to be the default clock of system. In the full fledge system, various type of sequences of clock are required for providing versatile segments. All of the sequences of clocks must be produced in between master clock & various other masking clocks.

G. Masking Clock

Masking clocks are implemented for masking of non-required clock pulses produced by master clock for providing power efficient sequence of clocks for some FFs.

H. Combinational Logic Circuit

Master& Masking clocks undergo the process in combinational logical circuitry that furnish the required sequences of clock. This segment operates like a system of gating of clock.

I. Series of Flip-flops

This section helps in execution of the main function of Johnson counter. The toggle operation for J-K FF (in which both of the inputs lies at 1) instead of shift registers methodology. All of the J, K inputs of FF are linked to VDD or either 1. Whenever a clock edge is require by a FF (positive edge for the FF triggered over positive edge), it will lead to variation in the values accumulated into it. A clock gating system is been developed for regulation of clock pulses in the FFs.

J. Output

This portion will generate outcome of Johnson Counter. The outcome given by Johnson counter is presented in truth table in TABLE I (2 bit) & TABLE II (4 bit).

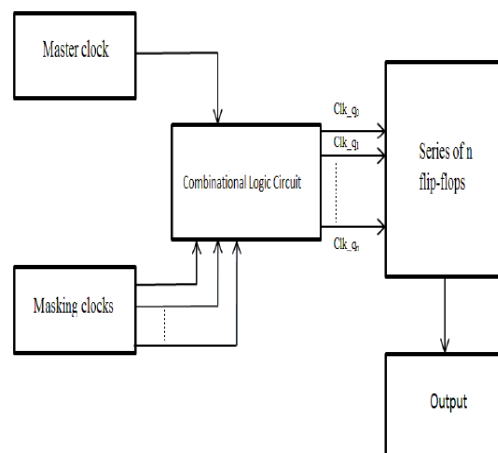


Figure 7: Block diagram of our proposed system

Table 3: Truth Table of 4-Bit Johnson Counter

State	Q3	Q2	Q1	Q0	Clock Pulse
S1	0	0	0	0	1
S2	1	0	0	0	2
S3	1	1	0	0	3
S4	1	1	1	0	4
S5	1	1	1	1	5
S6	0	1	1	1	6
S7	0	0	1	1	7
S8	0	0	0	1	8

We intend to design both of the 2-bit & 4-bit Johnson counter as per the designing schema. In this system, whenever is required, a clock pulse will be provided to the FF in order for toggling the value accumulated into it. Hence, there is no chance for non-affective transition of clock pulse whenever FF is kept in holding state. By this we are able to reduce the dissipation of power. Along with it, J-K FF is applied along with the toggle operation, so we can eliminate various interlinks. For e.g. last D-FF is linked to first FF inverted output links, various Ff connections. So the system turns out to be very convenient & effective to ensure that it has less number of interconnections & low dissipation of power.

II. PROBLEM STATEMENT

In the previous document [13], a Johnson counter using a basic D-FF is implemented. A basic D-type FF is also designed by using Johnson counter. As presented from the diagram, a combination of 12 transistors is used in the D-FF. In the combination, several transistors are being applied. Over the input data side & clk are applied while outcome of D-FF is obtained. This design of D-FF makes use of Johnson counter. Hence, as per the diagram aggregated absorption of power by transistor increases. So there is a need for minimizing the quantity of transistors on the D-FF CMOS circuitry for reducing the aggregated absorption of power.

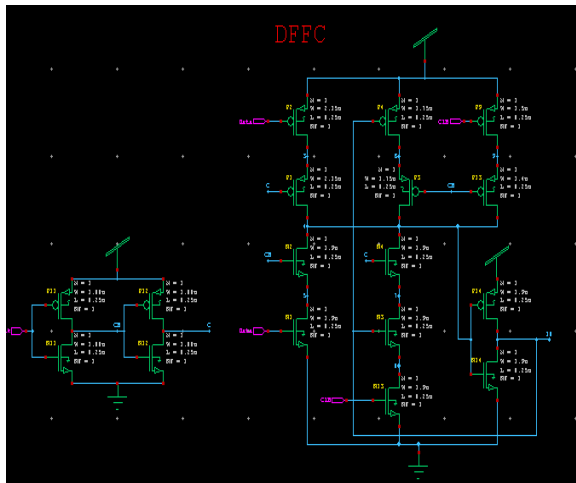


Fig 8: D flip flop CMOS circuit

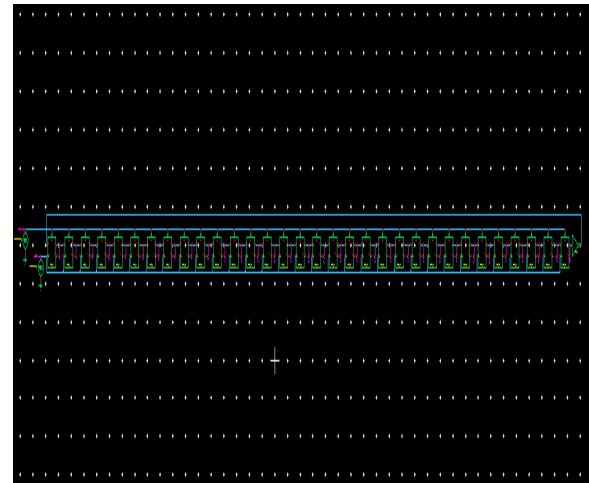


Fig 9: 32 bit Johnson counter

III. PROPOSED METHODOLOGY

In the suggested technology, we are working over minimizing the quantity of transistors on D-FF CMOS circuitry. From the diagram, it is observed that aggregated transistors are lessened. So it can be seen that suggested D-FF requires only 4 transistors. On the side of input, there are two inputs provided termed as (clk, d) while on the side of output, a single outcome is there as (q). Aggregated consumption of power is minimized because of fewer transistors. In the designed circuitry, VDD is taken as 1.2V. On the side of output, waveform for q1, q2, q3, q4, q5, q6, q7 counters is presented.

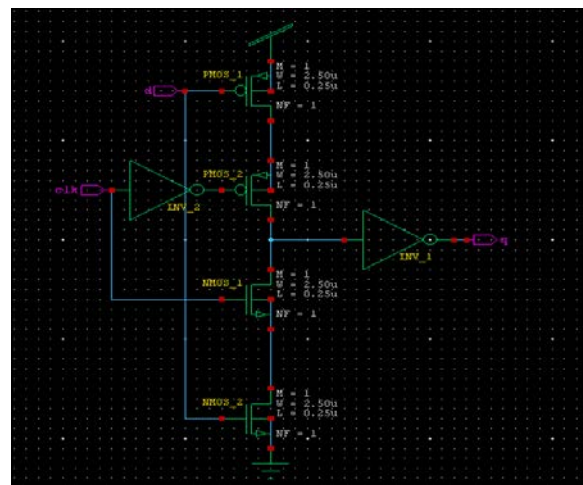


Fig 10: proposed D flip flop

For clock input, source of voltage of bit form is applied so the input can be given in the form of bits i.e. 0 & 1. In the Johnson counter input clock goes over while q0, q1, q2 outcomes are being obtained. The suggested counter works over 1.2V in form of VDD.

IV. RESULTS

A. Existing Design

In the project, a Johnson counter of 32 bit is designed that operates over 1.2V VDD. The input to clock is provided & outcome is obtained in the form of q0, q1, q2, q3, q4....q31 bits. It is observed from figure 4.1 a 32-D FF is linked up for designing of 32 bit Johnson counter.

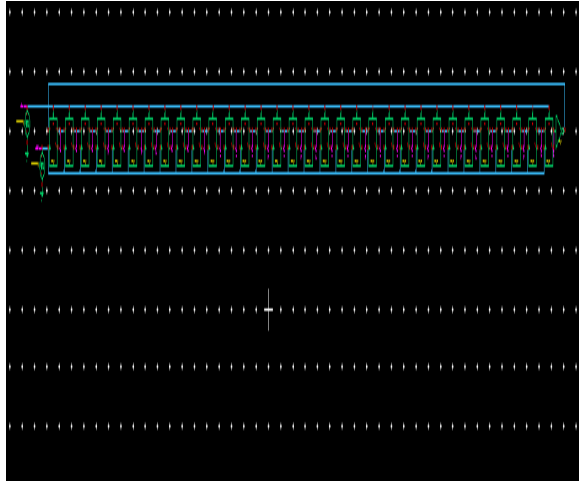


Fig 11: 32 bit Johnson Counter

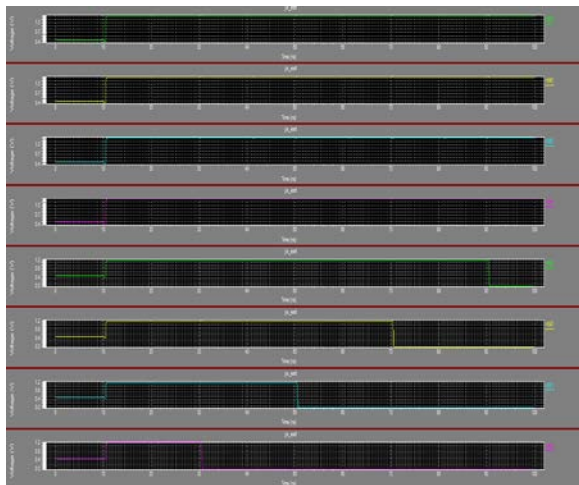


Fig 12: Output waveform for 32 bit Johnson counter

As from the waveform produced by outcome, the waveform for outcome of q0, q1, q2, q3, q4, q5, q6, q7 is presented. It is not possible to present all the 32 bits. In the base paper, consumption of power for the present design for a 32 bit Johnson counter is attained as 9.322139e-004W & delay is 840.06 ps.

B. Proposed 32 Bit Johnson Counter

In the project, a Johnson counter of 32 bits is been designed that operates over 1.2 V voltage supply. An

input for clock is provided & over the output side, the outcome obtained is of q0, q1, q2, q3, q4...q31 bits. As observed from figure, a 32-D FF is linked for designing of 32—bit Johnson counter.

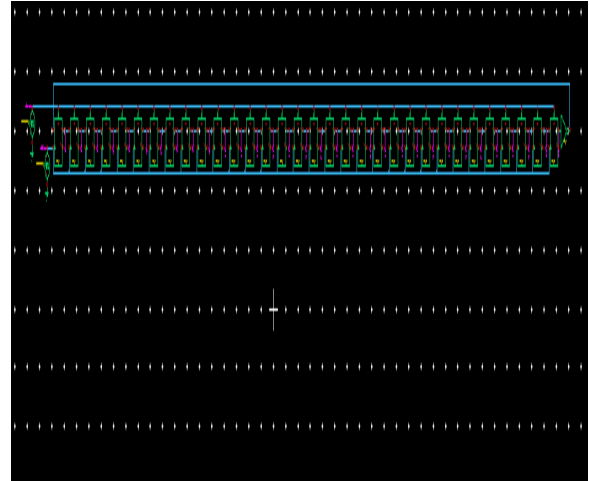


Fig 13: 32 bit Johnson Counter

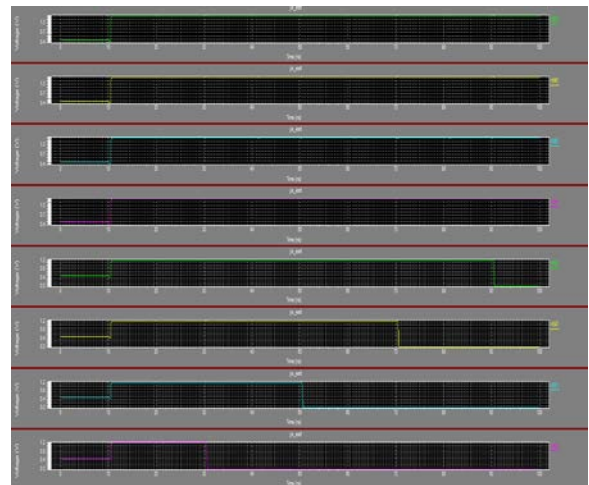


Fig 14:-Output waveform for 32 bit Johnson counter

As observed from waveform of outcome, the waveform for outcome q0, q1, q2, q3, q4, q5, q6, q7 is presented. It is not possible for presenting the outcome for all the 32 bits. In base paper, the consumption of power in present design is 1.791674e-004W where as delay is 504.04ps for 32 bit Johnson counter.

Table 4: Comparison table

	Power (W)	Delay (ns)
Base paper	9.322139e-004	840.06ps
Proposed Design	1.791674e-004	504.04ps

V. CONCLUSION AND FUTURE SCOPE

A. Conclusion

The suggested design is more efficient & noteworthy than the traditional designs while taking the dissipation of power into account because of simplified interlinks & clock changeovers. In a state of dissipation of power, the observation is concentrated on dissipation of power because of transitions of clock as mainly these clock transitions are the reason behind power dissipation. It also seems that consumption of power & delay is minimized as the D-FF is transformed with minimal quantity of transistors.

B. Future Scope

With further development, methodology of GDI is implemented for improvisation in performance of power. By the minimization in the length of channel, the delay of system can be reduced.

REFERENCES

1. M. Pedram, "Power minimization in IC design: Principles and applications", ACM Trans. Design Automation, vol. 1, no. 1, pp. 3- 56, Jan. 1996
2. Neil H. E. Weste, David Harris and Ayan Banerjee, CMOS VLSI Design , 3rd edition, Dorling Kindersley Pvt. Ltd. 2006.
3. K. Roy and S. Prasad, "Circuit activity based logic synthesis for low power reliable operations", IEEE Transitions, VLSI Systems, 1(4):503-513, 1993.
4. E. Olson and S. Kang, "State assignment for low power synthesis using genetic logic local search", in IEEE Proc. Custom Integrated Circuit Conf., 140-143, May 1994.
5. L. Benini and G.D. Michel, "State assignment for low power dissipation", IEEE Journal of Solid-State Circuits, 30(3): 258-268, 1995.
6. Q. Wu, M. Pedram and X. Wu, "Clock gating and its application to low power design of sequential circuits", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 3(47), March 2000.
7. M. Pedram, Q. Wu and X. Wu, "A new design of double edge triggered flip-flops", In Proc. Of ASP-DAC, Yokohama, 417-421, February, 1998.
8. X. Wu, J. Wei and M. Pedram, "Low-power design of sequential circuits using a quasi-synchronous derived clock", in Proc. Of ASPDAC, Pacifico Yokohama, January 2000.
9. X. Wu and Massoud Pedram, "Low power sequential circuit design using priority encoding and clock gating", Power Electronics and Design, 2000. ISLPED '00. Proceedings of the 2000 International Symposium on, 143-148, July 2000.
10. S.H. Unger, "Double-edge-triggered flip-flops", IEEE transactions on Computers, 30(6): 447-451, 1981.
11. E. Macii, M. Pedram and F. Somenzi, "High level power modeling, estimation and optimization", IEEE Transactions on Computer Aided Design, 17(11): 1061-1079, 1998.
12. Thomas L. Floyd, Digital Fundamentals, Pearson education, Inc., 2003, edition: 2009-2010.
13. Sani M. Ismail, Saadmaan Rahman, Mohammed M. Rahman and Neelanjana S. Ferdous , " A Design Scheme of Toggle Operation Based Johnson Counter with Efficient Clock Gating