

Design and Optimization of 64-Bit Carry Select Adder using TG Technology

Gurpreet Kaur¹, Er. Hardeep Singh²

Post graduate student, Dept of ECE, BFCET, Bathinda, India (gkpreetkaur808@gmail.com)¹,

Head of Department of E.C.E., BFCET, Bathinda, India (hodece.bfcet@gmail.com)²

Abstract

Many computers and other kinds of processors the adder is the most commonly used arithmetic block. Adder is used in the arithmetic logic units, and also in other parts of the processor, where it is used to calculate addresses, table indices, and similar operations. In this paper, we proposed an area-efficient and high speed carry select adder that also having moderate power consumptions. In this paper, we implemented the carry select adder (CSA) without using multiplexer (MUX) for final selection. The MUX stage replaced by the use of combinational gates. The proposed architecture then compared with the carry select adder having two mux and the carry select adder having one mux. The 64-bit CSA, implemented using TG technology at 1.8 V voltage supply, provides 82% better Power-Delay-Product results when compared with CSA having MUX at 180nm technology.

Keywords: carry select adder, area efficient, high speed

I. INTRODUCTION

Addition is the most fundamental arithmetic operation, performed in digital circuits and processors, widely impacts the overall performance of processing elements. An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system [12]. The Ripple Carry Adder has a simple adder design, but carry propagation delay (CPD) is the main disadvantage of this type of adders. So Carry look-ahead Adder and Carry Select methods have been suggested to overcome the problem of simple adders.

The conventional Carry Select Adder consists of an RCA-RCA configuration with multiplexer. Addition of two n-bit numbers generates a pair of sum and carries output bits, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the final sum, as well as the final carry, is then selected with the multiplexer once the correct carry is known. In 2002, a new concept of hybrid adders is presented to speed up addition process by Wang et al. that gives hybrid carry look-ahead/carry select adders design [3]. In 2004, power-delay product minimization of 64-bit carry-select adders intended for high-performance and low-power applications, in 0.18- μ m partially depleted (PD) silicon-on-insulator (SOI), using complex branch-based logic (BBL) cells [1]. Ramkumar and Kittur suggested a binary to BEC-based CSLA. The BEC-based CSLA involves less logic resources than the conventional CSLA, but it has marginally higher delay [4]. A CSLA based

on common Boolean logic (CBL) is also proposed in [5]. The CBL-based CSLA involves significantly less logic resource than the conventional CSLA but it has longer CPD. In 2014, Mohanty and Patel proposed a logic formulation for the CSLA. The main contribution in this brief is logic formulation based on data dependence and optimized carry generator (CG) and CS design [12]. According to literature review, there is always a trade-off between area, delay and power parameters of VLSI. We proposed an area-efficient and high speed Carry Select Adder by reducing transistor count and achieve lower Power Delay Product (PDP).

The rest of the paper organized as follows. In Section II deals with the introduction about Conventional Carry Select Adder. Section III presents structure of Carry Select Adder by sharing common-boolean logic with two multiplexers. Sections IV and V deals with the introduction and structure of CSA using one multiplexer and proposed CSA without using multiplexer respectively. The simulation results and comparison among these adders analyzed in Section VI. Finally, the work is concluded in Section VII.

II. CONVENTIONAL CARRY SELECT ADDER

Carry select adder comes in the types of conditional sum adders. Conditional sum adders work on some conditions [13]. A carry-select adder generally comprises of two ripple carry adders (RCA) structure and with multiplexer. Addition of two n-bit numbers with a carry-select adder is performed with two ripple carry adders that perform the calculation twice, one time with $C_{in}=0$ and other

time assuming $C_{in}=1$. When these two results are calculated, the correct sum, and the correct carry, is selected with the use of multiplexer once the correct carry is known.

The carry select adder divides the ripple carry adder into M parts, while each part consists of a duplicated (N/M)-bit two carry ripple adders [5]. From these two carry ripple adders, one is calculated for carry input value is logic "0" i.e. $C_{in}=0$ and another ripple carry adder is

calculated for carry input value is logic "1" i.e. $C_{in}=1$. When their actual carry input is ready, the result of carry input value "0" path or the result of carry value "1" path is selected by the multiplexer according to its correct carry input value. The figure 1 shows 16-bit carry select adder is divided the carry ripple adder into 4 parts, while each part consists of a duplicated 4-bit carry ripple adder pair.

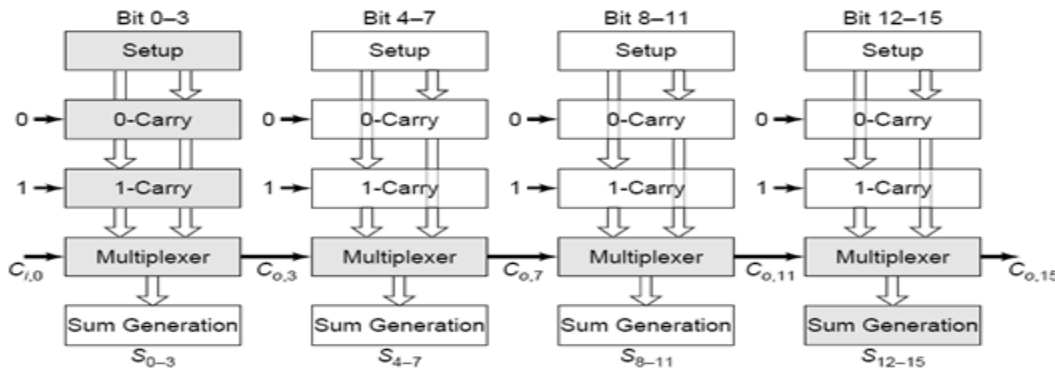


Fig. 1 The 16-bit carry select adder is divided the carry ripple adder into 4 parts, while each part consists of a duplicated 4-bit carry ripple adder pair.

III. CARRY SELECT ADDER WITH TWO MULTIPLEXERS BY SHARING COMMON BOOLEAN LOGIC

A conventional CSA has less CPD than an RCA, but has large area because the use of dual RCA. The main idea of this work is to remove the duplicate adder cells in the conventional CSA by sharing Common Boolean Logic (CBL) term [5]. Through analysing the truth table of a single-bit full-adder, it is easy to find out that the output of summation signal as carry-in signal is logic "0" is the inverse signal of itself as carry-in signal is logic "1". So is "0110" as C_{in} is logic "0" and S_0 is "1001" as C_{in} is logic "1".

Table 1: the truth table of one-bit full adder, where the upper part is case of $C_{in}=0$ and lower part is the case of $C_{in}=1$.

C_{in}	A	B	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

To share the common Boolean logic term, there is only need to implement one XOR gate and one INV gate to generate the summation signal pair. As actual carry-in signal is ready, the correct summation output signal is selected according to the logic state of carry-in signal. As for the carry propagation path, one OR gate and one AND gate are needed to count possible carry input values in advance. Once the carry-in signal is ready, the selection of the correct carry-out output is done according to the logic state of input carry signal. The figure 2 shows area-efficient carry select adder with common Boolean logic sharing.

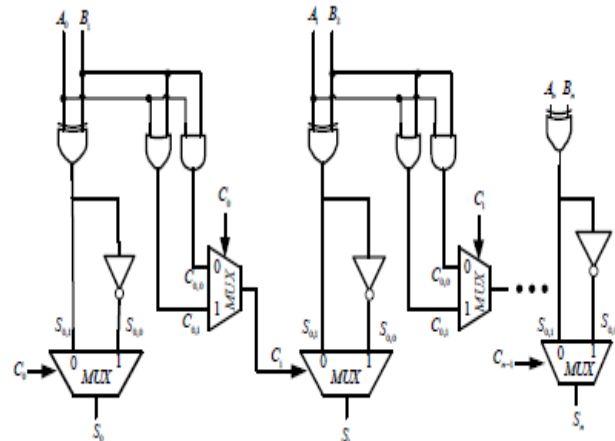


Fig. 2 Internal structure of the carry select adder is constructed by sharing the common Boolean logic term using two multiplexers.

The carry select adder by sharing common Boolean logic has less transistor count as compared to conventional CSA and achieve lower power delay product.

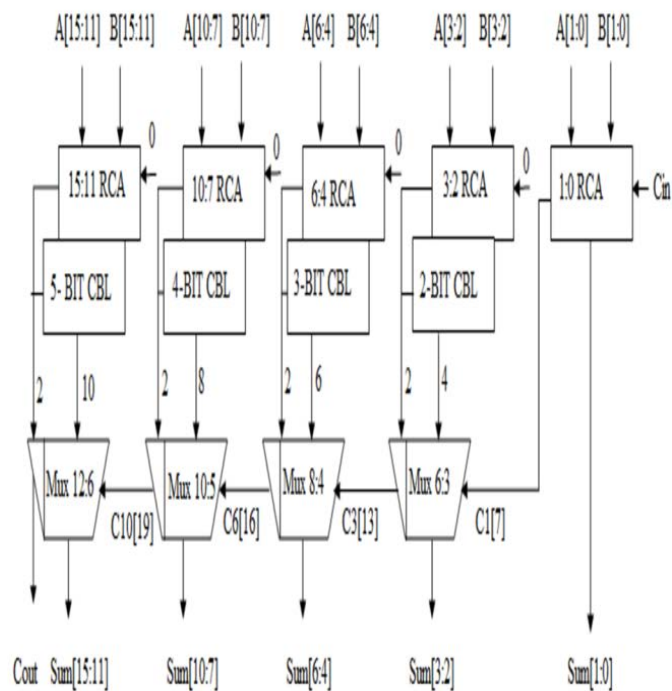


Fig. 3 16-Bit Proposed Sqrt CSLA using Common Boolean Logic

IV. CSA WITH ONE MULTIPLEXER BY SHARING COMMON BOOLEAN LOGIC

The duplicate adder cells of conventional carry select adder are removed in an area efficient CSA by sharing Common Boolean Logic (CBL) term using two multiplexers [11]. In another way, it is possible to reduce the gate count by replacing one multiplexer with another Ex-OR gate. There is need of multiplexer only for the correct carry output selection not for the selection of summation output. In this way, the gate count and power consumptions are reduced that is beneficial in VLSI applications. So there is a need only two Ex-OR gate or summation operation and two AND gates for carry output generation and then one multiplexer is used to select correct carry when input correct carry is known. The RCA circuit having Ex-OR gates is used to calculate for summation operation and the circuit having AND gates and multiplexer is used to generate and select the correct carry output operation respectively. The power consumptions, area and delay are reduced to large extent in this way with the use of only one multiplexer. The figure 4 shows the block diagram of carry select adder using one multiplexer for one-bit.

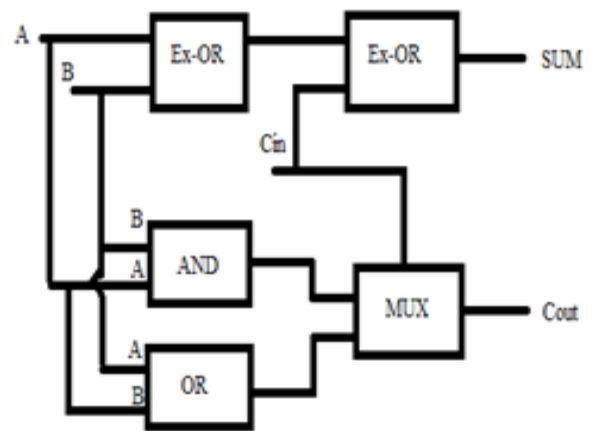


Fig. 4 Block diagram of CSA with one MUX

The carry select adder using one multiplexer developed for 64-bit position provides better results over carry select adder using two multiplexer in terms of area, power and delay.

The figure 5 shows the internal schematic structure of carry select adder by using one multiplexer only

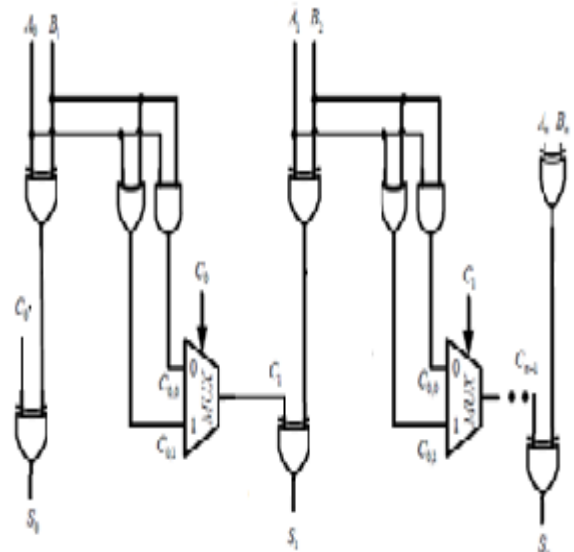


Fig. 5 Internal structure of the carry select adder is constructed by sharing the common Boolean logic term using one multiplexers.

V. PROPOSED CSA WITHOUT USING MULTIPLEXER

In this paper the carry select adder is proposed that mainly focus on to improve the performance of adder with reduced area, high speed and low power consumption. In digital adder circuits, the speed of addition is limited by the time required for a carry to propagate through the adder. Carry Select Adder (CSA) is used to solve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the final sum.

In this method the multiplexer is replaced by the simple combinational circuit which consists of Ex-OR and AND gates. By using this method area and delay is reduced when compared to previous discussed carry select adders i.e. CSA with two MUX and CSA with one MUX. Initially RCA structure is calculate for $c_{in} = 0$ the output of full adder is givento the combinational circuit and one of the input of that combinational circuit is previous stage carry then it will provide the proper output by using Ex-OR and And gates structure. In this way, area is reduced to such a large extent because to implement the full adder design we need only two Ex-OR gate, two AND gates and one OR gate. All the gates are implemented using TG Technology. In this way the gate count or area of the full adder design is reduced to large extent. The figure 6 shows the block diagram for 16-bit carry select without using multiplexer. The multiplexer replaced by the combinational circuit.

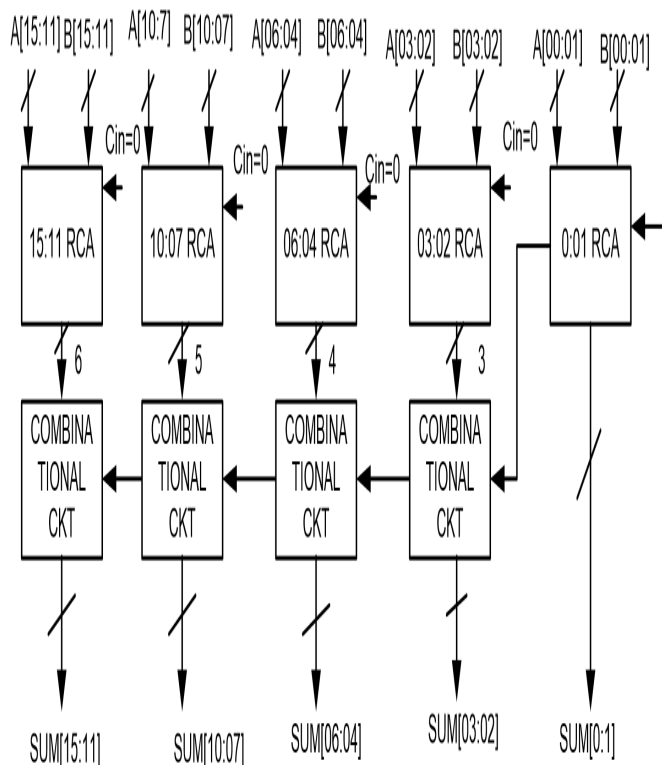


Fig. 6 CSA without using multiplexer

The figure 7 shows the internal structure for CSA without using MUX. This is the schematic pattern of gates used in the adder design. Where A, B, C_0 are the initial three inputs for full adder and output sum and output carry of first stage denoted as S_0 and C_1 respectively. This work

extended to 64-bit position for final results and compared with other existing architectures.

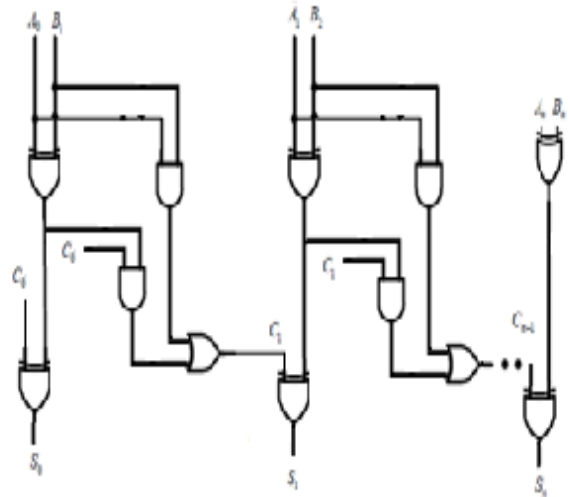


Fig. 7 The internal structure of carry select adder without using multiplexer.

The carry select adder without using multiplexer is developed for 64-bit position that provides better results in area and delay parameters of VLSI and also lower Power Delay Product as compared with previous architectures

VI. TANNER TOOL SIMULATION RESULTS

The work has been developed using Tanner Tool version 7. The architectures are proposed for 64-bit position using TG Technology. The transistor count of our area-efficient carry select adder could be reduced to be very close to that of carry ripple adder, the transistor count in the conventional carry select adder is nearly double as compared with the proposed design.

The area-efficient carry select adder achieves an outstanding performance in area and delay parameters. We simulated the designs of 64-bit position using TANNER Tool with 64-bit in 0.18 μm CMOS technology. The figure 8(a) shows the schematic diagram of CSA with two MUX for one-bit position in tanner tool window. The figure 8(b) shows the schematic diagram of one-bit CSA with one MUX only having reduced gate count. The figure 8(c) shows the schematic diagram of CSA without using MUX for one-bit wide in tanner tool window having reduced gate count as compared to previous both designs. This work extended to 64-bit position of full adder.

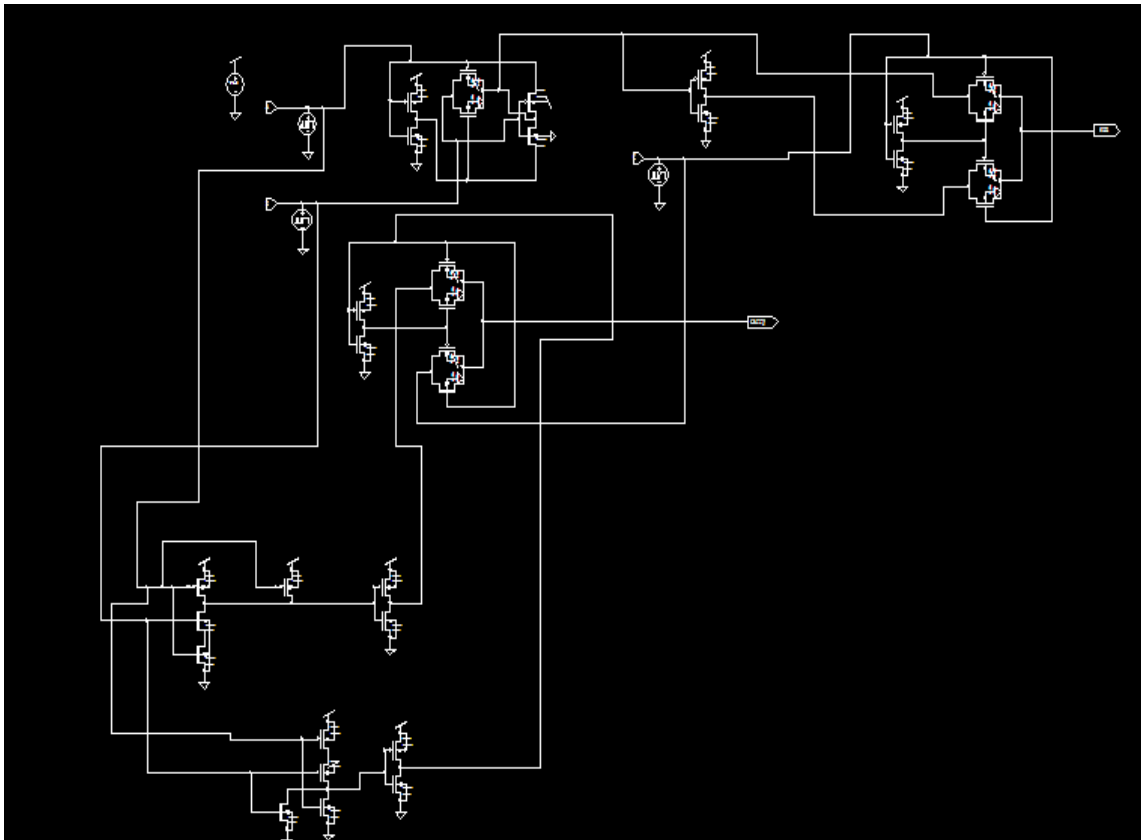


Fig. 8 (a) Schematic pattern for CSA with two MUX for one-bit position.

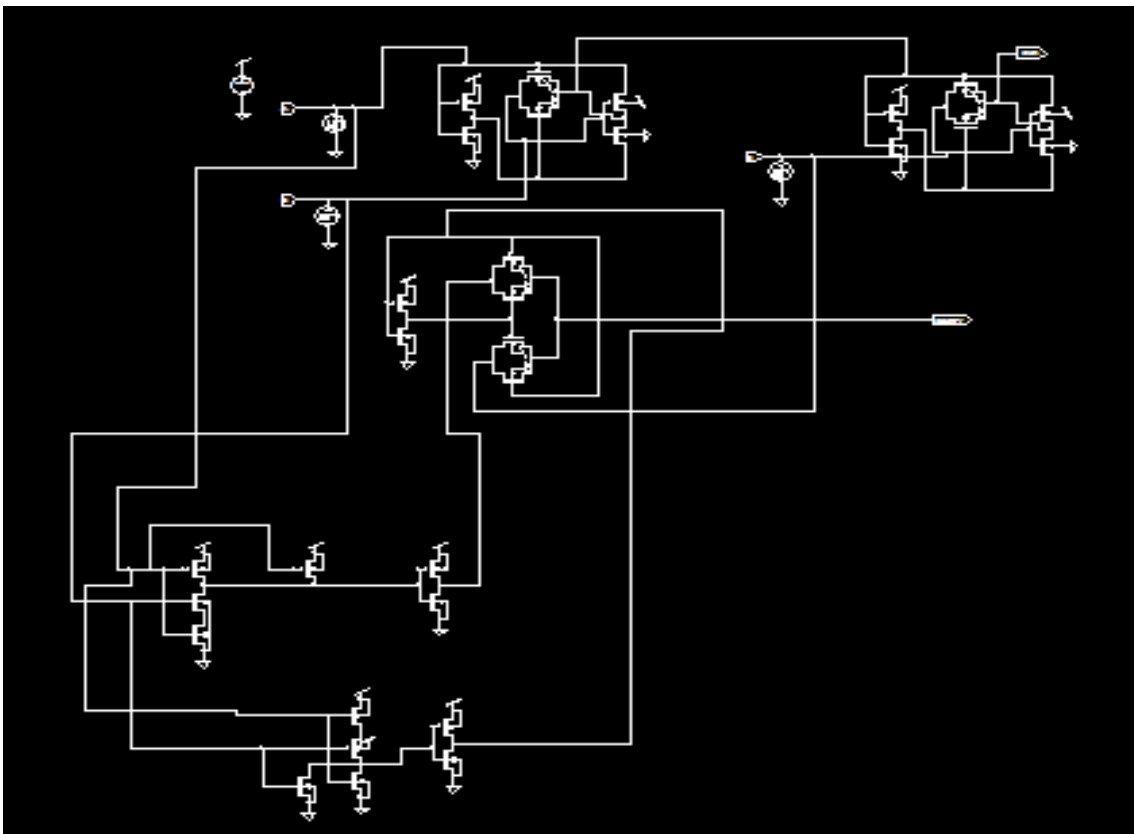


Fig. 8(b) Schematic pattern for CSA with one MUX for one-bit position.

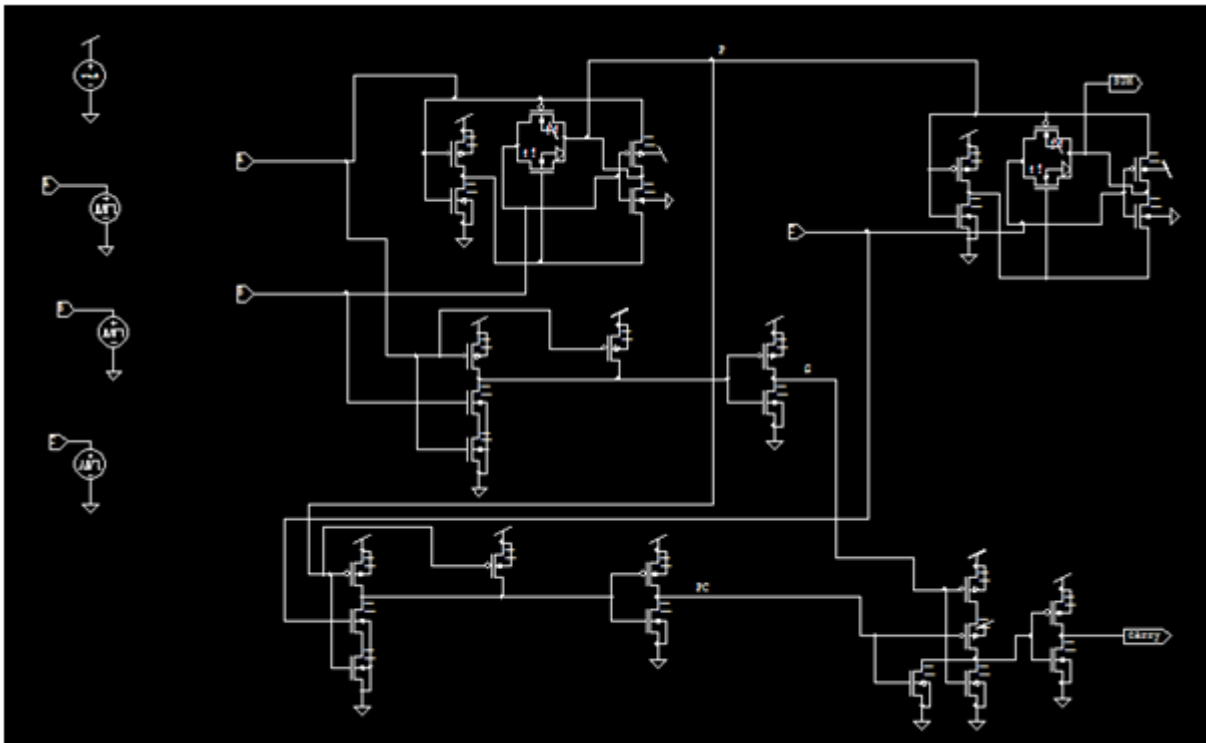


Fig. 8(c) Schematic pattern for one-bit CSA without using MUX.

The figure 9 shows the output waveform for 64-bit CSA without using MUX. In this there is three inputs a, b, and c and outputs are sun and carry. The figure shows results in waveform-edit of Tanner tool.

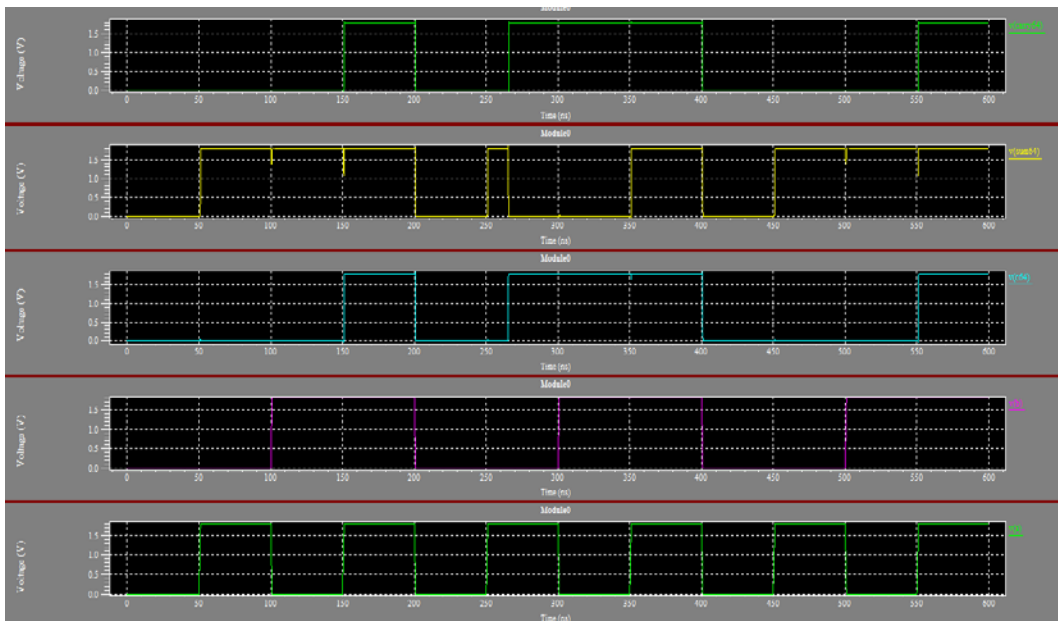


Fig. 9 Waveform pattern for 64-bit CSA without using MUX.

The table 2 shows the comparative results analysis for CSA with two MUX, CSA with one MUX and CSA without using MUX. The compared results show that the area efficient carry select adder has less delay, reduced area, lower power consumptions and lower power delay product. The results are simulated by using TANNER Tool version 7. All designs are 64-bit wide using TG Technology. The width of NMOS and PMOS is taken 16 μ m and 42 μ m respectively. The supply voltage used is 1.8 V.

Table 2 simulated results comparison table for three designs of Carry Select Adder.

Design	CSA with 2 MUX	CSA with 1 mux	CSA without MUX
No. of transistors	2242	2112	1440
Technology file (nm)	180	180	180
Power consumptions (mw)	15.1381	5.7241	6.4725
Delay at sum (ns)	0.4014	0.2796	0.0564
Delay at carry (ns)	0.1701	0.1826	0.0723
Power Delay Product (pJ)	2.5749	1.0452	0.4679

Figure 10 shows the percentage reduction comparison over three designs of carry select adder i.e. CSA using two MUX, CSA using one MUX and CSA without using MUX. CSA using one multiplexer consumes less area than CSA with two MUX. CSA without using multiplexer has great advantage in terms of area and delay as compared to both. Power delay product of CSA with 1 MUX is 55% better than CSA using 2 MUX. PDP of CSA without MUX is 82% and 55% better than CSA using 2 MUX and CSA using 1 MUX respectively for 180 nm technology file. Figure 10(a), 10(b), 10(c) and 10(d) shows comparison over area in number of transistors, power consumptions, delay and Power Delay Product (PDP) respectively.

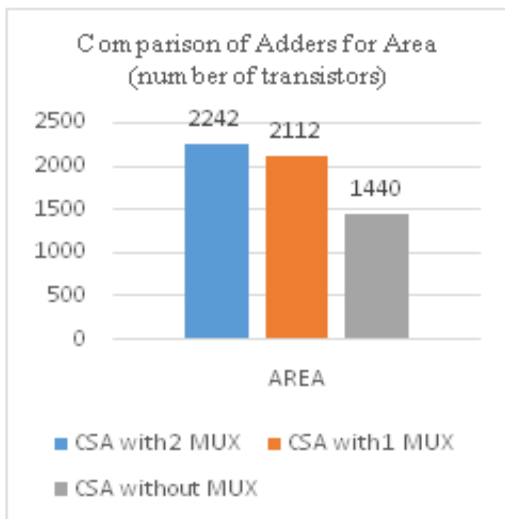


Fig. 10(a) Comparison of adders for Area.

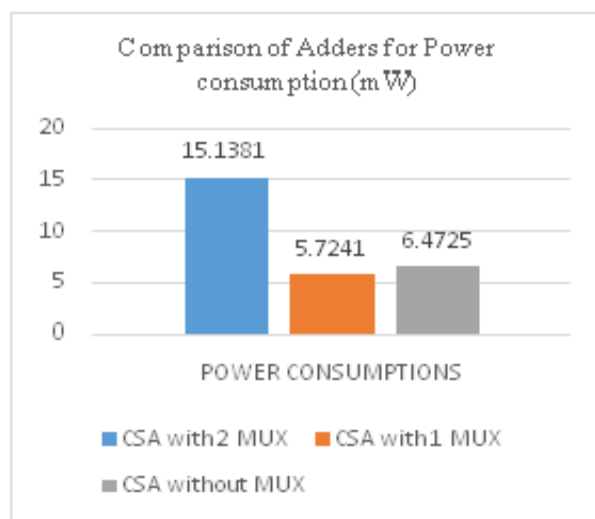


Fig. 10(b) Comparison of adders for Power consumptions.

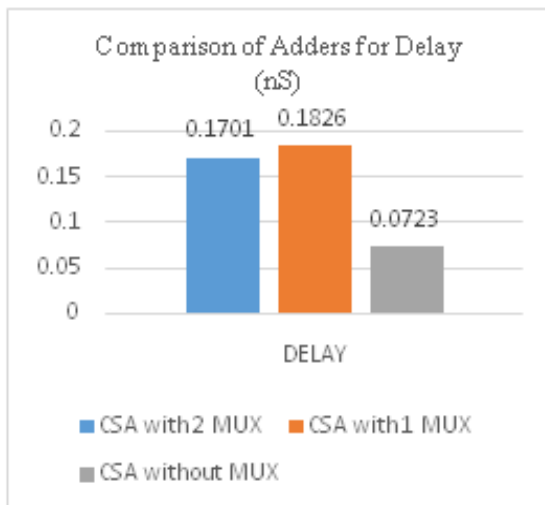


Fig. 10(c) Comparison of adders for Delay.

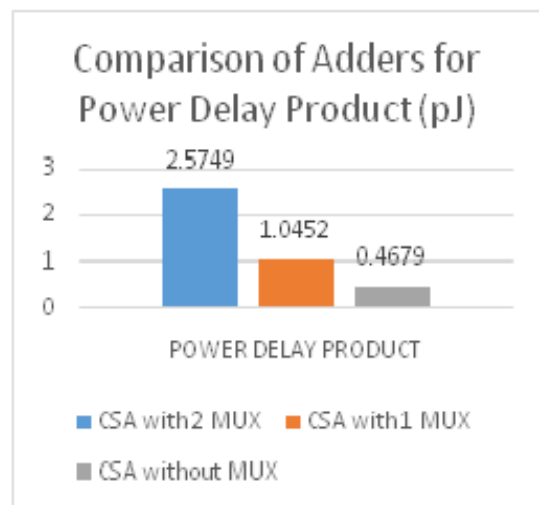


Fig. 10(d) Comparison of adders for Power Delay Product.

VII. CONCLUSION

Two architectures, Carry Select Adder (CSA) using only one multiplexer and carry select adder without using multiplexer, are developed and compare with recently proposed carry select adder architecture by sharing common Boolean logic, using two multiplexers. CSA using one multiplexer consumes less area than CSA with two MUX. CSA without using multiplexer has great advantage in terms of area and delay as compared to both. Power delay product of CSA with 1 MUX is 55% better than CSA using 2 MUX.

PDP of CSA without MUX is 82% and 55% better than CSA using 2 MUX and CSA using 1 MUX respectively for 180 nm technology file.

VIII. FUTURE WORK

- TG Based advanced full adder circuit reduces the transistor count, power consumption and delay of the circuit. The work of this project may be further extended by various ways as:
- The work can be extended to higher bits of adders (128-bit).
- The work can be extended to change the technology file by optimization of the parameters like frequency, length, width etc.
- The efforts can be made to decrease the transistor count so further Power, area and delay by changing the parameters.

Research steps can be taken by using the other types of adders like Ripple Carry Adder, Hybrid adder etc.

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