ISSN: 2348 - 2117

International Journal of Engineering Technology and Computer Research (IJETCR)
Available Online at www.ijetcr.org
Volume 3; Issue 4; July-August-2015; Page No. 205-208

# Analyzing the Implementation of a NoC Performance Simulation Framework

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**Abstract**

NOC architectures are based on packet-switched networks. To extend the applicability of moore's law, the Multiprocessor architectures and platforms have been introduced. They depend on concurrency and synchronization in both software and hardware to enhance the design productivity and system performance. To design and implement network- on- chip simulation framework for supporting 3-D Mesh, Irregular and 2-D NoC. The simulation framework is proposed to be capable of evaluating the performance of various topology designs and routing function based on popular communication performance matrices such as Latency, Throughput, and Energy etc.

**Key words: NOC, SOC, IC, Simulation Framework, Mesh.**

## 1. Introduction

On a billion transistors chip, it may not be possible to send a global signal across the chip within real-time bounds. If the SoC (System-on-Chip) is synchronized by a global clock signal, the circuit will be more prone to EMI (electromagnetic interference) [2]. The traditional system designs are usually based on critical paths and clock trees. These critical paths and clock trees contribute to an increased amount of power consumption. Therefore, SoCs are not power efficient. Besides, it is difficult to manage these clock trees due to clock skew problems [3]. Network-on-Chip (NoC or NOC) is an approach to designing the communication subsystem between IP cores in a System-on-a-Chip (SoC). NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. The wires in the links of the NoC are shared by many signals. A high level of parallelism is achieved, because all links in the NoC can operate simultaneously on different data packets. Therefore, a NoC provides enhanced performance (such as throughput) and scalability in comparison with previous communi-cation architectures (e.g., dedicated point-to-point signal wires, shared buses, or segmented buses with bridges). The project aims to utilize the benefits of increased throughput by network on chip designs. The project uses NIRGAM simulator to implement NoC. Nirgam simulator is designed in systemC which is the class library of C++.The Nirgam simulator implements the 2D NoC topologies basically. But the 3D NoC has several benefits over 2D NoC.

## 2. Literature Survey

NOC architectures are based on packet-switched networks. This has led to new and efficient principles for design of routers for NOC [10]. Assume that a router for the mesh topology has four inputs and four outputs from/to other routers, and another input and output from/to the Network Interface (NI). Routers can implement various functionalities - from simple switching to intelligent routing.

With the development of IC technology and the increasing processing, power requirements, more and more processing cores are integrated into one single chip. One of the key problems is the communication efficiency between the processing cores. The network on chip (NoC) has been proposed as a solution for the communication challenge.

It uses packet based scheme to forward messages in an on-chip communication network instead of dedicated wires connection. These are based on networks instead of using traditional buses or peer to peer connections. The structured network wiring gives well controlled electrical parameters that eliminate timing iterations and enable the use of high performance circuits to reduce Latency and increase Bandwidth. Using a network to replace global wiring has advantages of structure, performance and modularity (Ogras, 2005). With this approach, system modules (processors, memories, peripherals, etc.) communicate by sending packets to one another over the network. In NoC, nodes are arranged in the topology such that communication between any nodes is possible even though they are not directly connected. Each node is a IP core which can be a DSP, Microprocessor, Memory or a Router, that is



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responsible for forwarding the data packet to the neighboring node. Each IP is placed in a rectangular tile on the chip and communicates with all other IP, not just with its neighbors, but also to any other IP on the chip via the network. Using a network to replace global wiring has advantages of structure, performance, better predictability, low power consumption and scalability as compared to traditional bus based systems.

This generic, modular and extensible frame work provides substantial support to experiment with NoC designs in terms of routing algorithms, application on various topologies and related performance parameters (Ogras,2005). Since NoC technology decouples communication from computation, on-chip communication modules can also be reused like computation IP's, hence helps to improve the design productivity. The importance of our proposed framework is that we can evaluate network design based on various performance metrices for a given set of choices.

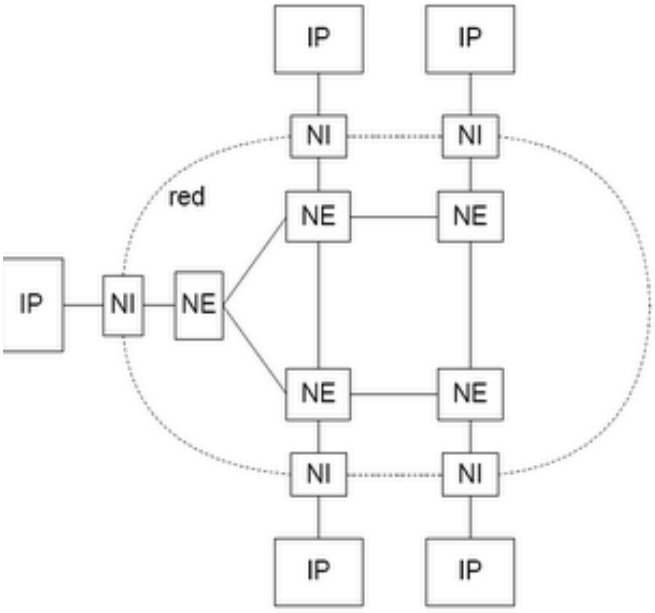


**Fig 1: Communication Infrastructures in NoC**

A common workflow of an application-specific networks-on-chip design includes network topology synthesis, communication channel width and buffer size selection, IP core mapping, packet routing and switching, and real-time scheduling of the task executions and communication. The communication infrastructures based in NoC has Network Elements (NE) and Network Interfaces (NI). The Packet travel across the Network Elements while the Network Interfaces provide an interface with the IP.

- **Platform Applicability**

C and C++ are being used as ad-hoc modeling languages and its model simulated to verify functionality. Many NoC Simulators such as Wormsim , VNOC, Siscosys were written in C++.

Our proposed research will consist of a Network simulator which will be written using SystemC language. For our proposed work, systemC will be installed on Ubuntu enviroment. SystemC is nothing but a a C++ class library and methodology that can effectively be used to create a cycle-accurate model of a system consisting of software, hardware and their interfaces. SystemC is a system design language that has evolved in response to pervasive need for a language that improves overall productivity for designers of electronic systems (M. Milliberg, 2004). SystemC offers real productivity gains by letting engineers design both the hardware and software components together for the final system, but at a high level of abstraction. This higher level of abstraction gives the design team a fundamental understanding early in the design process of the intricacies and interactions of the entire system and enables earlier verification, and overall productivity gains through reuse of early system.

Our proposed NoC Simulator aims to provide researchers with efficient mechanism to experiment with NoC design in terms of routing algorithm and applications on various topologies.

**3. Detailed NoC Simulation Framework Architecture design**

The NOC architecture provides the communication infrastructure for the resources**.** The NOC architecture is a m × n mesh of switches and resources are placed on the slots formed by the switches. Each switch is connected to one resource and four neighboring switches, and each resource is connected to one switch. A resource can be a processor core, memory, an FPGA, a custom hardware block or any other intellectual property (IP) block, which fits into the available slot and complies with the interface of the NOC. The NOC architecture essentially is the On chip communication infrastructure comprising the physical layer, the data link layer and the network layer of the OSI protocol stack. We define the concept of a region, which occupies an area of any number of resources and switches. This concept allows the NOC to accommodate large resources such as large memory banks, FPGA areas, or special purpose computation resources such as high performance multi-processors.

The concrete architecture of NoC Simulation framework that defines the number of switches and

shape of the network, the kind and shape of regions and the number and kind of resources. The applications are mapped onto the concrete architecture to form a concrete product. The simulation phase covers the necessity of obtaining the NoC communication infrastructure suited for a particular application. This phase will increase the efficiency by selecting the appropriate parameters, allowing a better latency and throughput.

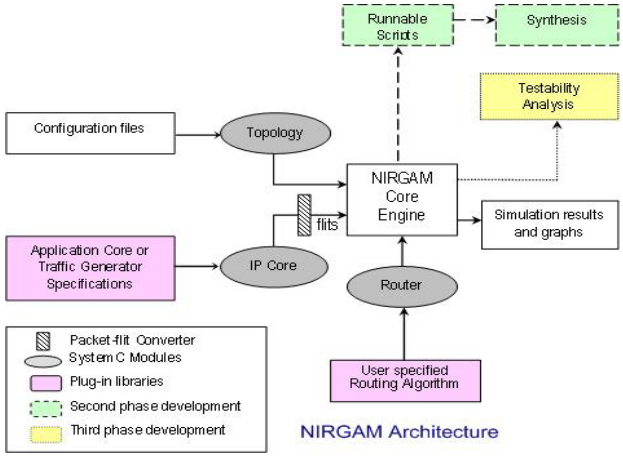


**Fig 2: Detailed NoC Simulation Framework Architecture design**

Topology and NoC specific parameters are read from configuration files. Application and router libraries are attached to tiles dynamically as per user configuration. Results and log files are created as per user specifications after simulation.

**4. NoC Simulation Framework Implementation**

Many NoC Simulators have been proposed and are being currently used by the NoC Research community. Noxim, Nostrum, BookSim are some simulators. Our proposed research will consist of a Network simulator which will be written using System C language on a Ubuntu environment The objective of our proposed work is to design and implement network-on-chip simulation framework for supporting 3-D Mesh, Irregular and 2-D NoC. The Simulation is proposed to be generic and upgradable in nature to facilitate the NoC Research Community to upgrade and customize the framework according to the Design needs. The simulation framework is proposed to be capable of evaluating the performance of various topology designs and routing function based on popular communication performance metric such as Latency, Throughput and Energy etc. The proposed framework will support both the Regular and Irregular topology. The output can be seen using Gnu Plot or Mat lab.

**5. Analyzing Benefits of 3D NoC over 2D NoC**

1. For same number of nodes, diameter of three dimensional Network-on-Chip (3D NoC) is less than that of 2D NoC.
2. 3D-NoC is potentially promising and emerging design paradigm wherein diameter reduction may lead to an improved throughput and reduced latency.
3. 3D NoC has lower dissipation of energy as compared to 2D-mesh topology.

The project aims at designing the 3D mesh topology on Nirgam simulator and designing the XYZ routing algorithm.A 3D-NoC is the stack of 2D-NoC in such a way that each stack is again connected to its front and rear stack. Figure 3. shows the corresponding 4x4x4 3D-Mesh topology constituted of four 4x4 2D-Mesh NoCs stacked to the rear.

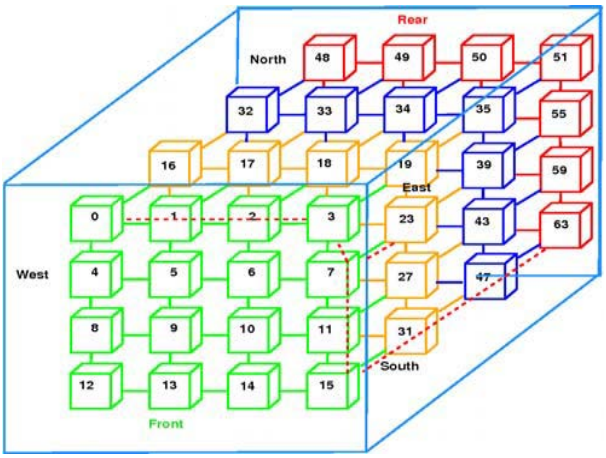


**Fig 3: Showing 4x4x4 3D-Mesh NoC**

The structure of a tile in 3D mesh NoC is as shown in figure below.

**6. Conclusion**

A simulation environment must allow us to integrate hundreds of cores and model concurrency and synchronization issues. This requires the representation of various activities and algorithms with appropriate MoCs (Models of Computation). To design and implement network- on- chip simulation framework for supporting 3-D Mesh, Irregular and 2-D NoC. The Simulation is proposed to be generic and upgradable in nature to facilitate the NoC Research Community to upgrade and customize the framework according to the Design needs. The simulation framework is proposed to be capable of evaluating the performance of various topology designs and routing function based on popular communication performance mertric such as Latency, Throughput and Energy etc.

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