

A Digital CMOS Implementation with Power Dissipation

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Abstract

The power dissipation source of CMOS circuits is presented. Specifically, the main principles of Inversion Duality dynamic, static, Charging and Discharging of Load Capacitances and leakage power dissipation Short-circuit Power Dissipation are illustrated together with the low power strategies for reducing each power component.

Keyword: Digital, CMOS, PMOS, NMOS Static, Dynamic, Power, Function.

1. Introduction

CMOS is also sometimes referred to as complementary-symmetry metal-oxide semiconductor (COS-MOS). The words "complementary-symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs and n-type metal oxide semiconductor field effect transistor for logic functions [3,7]. Two important characteristic of CMOS devices are high noise immunity and low static power consumption. Since, one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between ON and OFF states. The phrase "Metal-oxide semiconductor" is a reference to the physical structure of certain field-effect transistor having a metal gate electrode placed on the top of an oxide insulator. The following section illustrates an overview of CMOS technology.

2. CMOS Technology Overview

CMOS refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. CPU's with best performance per watt each year have been CMOS static logic. CMOS circuits use a combination of p-type and n-type metal-oxide-semiconductor field effect transistor to implement logic gates and other digital circuits. A basic circuit arrangement of CMOS inverter is shown in Fig.

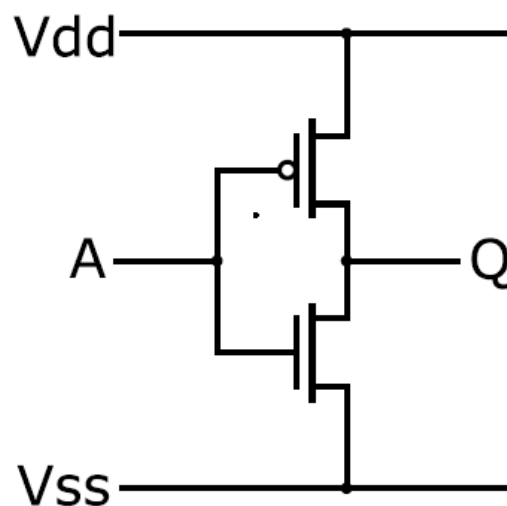


Figure 1: A CMOS inverter

2.1 Inversion

CMOS circuits are constructed in such a way that all PMOS transistor must have either an input from the voltage source or from another PMOS transistor. All NMOS transistor have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. The composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied. CMOS accomplishes current reduction by complementing every NMOS with a PMOS and connecting both gates and both drains together [1]. A high voltage on the gates will cause the NMOS to conduct and PMOS not conduct while a low voltage on gates causes reverse operation. This circuit arrangement

greatly reduces power consumption and corresponding heat generation.

When an input is connected to both a PMOS transistor and an NMOS transistor. When the voltage of input of A is low, the NMOS transistors channel is in a high resistance state. This limits the current that can flow from Q to ground. The PMOS transistor's channel is in a low resistance state and much more current can flow from the supply to the output because the resistance between the supply voltage and Q is low, the voltage drop between the supply voltage and Q is low, the voltage drop between the supply voltage and Q due to a current drawn from Q is small. The output low for registers a high voltage [6].

On the other hand, when the voltage of input A is high, the PMOS transistor is in an off (high resistance) state so it would limit the current flowing from the positive supply to the output while the NMOS is an ON state (low rise) state, allowing the output from drain to ground. Because, other resistance between Q and ground is low, the voltage drop due to a current drawn into Q placing Q above ground is small. This low drop results in the output registers a low voltage. The power supply for CMOS is called VDD and VSS or VCC and ground (GND) depending on the manufacturing. VDD and VSS or VCC are carry over's from conventional MOS circuits and stand for the drain and source supplies.

2.2 Duality

An important characteristic of a CMOS circuit is the Duality that exists between its PMOS transistors and NMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground. To accomplish this, the set of all paths to the voltage source must be the complement of the set of all paths to ground [2]. This can be easily accomplished by defining one in terms of the NOT of the other. Due to De Morgan's laws based logic, the PMOS transistors in parallel have corresponding NMOS transistor in series while the PMOS transistor in series have corresponding NMOS transistors in parallel[3].

3. Power Dissipation

CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching (dynamic power). On a typical ASIC in a modern 90 nm process, switching the output might take 120 picoseconds and happens one every ten nanosecond. NMOS logic dissipates power whenever transistor is ON because there is a current path from VDD to VSS through the load resistor and the n-type network. Static CMOS gates are very power efficient because they dissipate nearly zero power when idle.

Earlier, the power consumption of CMOS devices was not the major concern while design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously.

3.1. Static Power Dissipation

If we consider a static CMOS inverter, when the input= '0', the associated NMOS transistor is OFF and the PMOS transistor is ON. The output voltage is V_{DD} or logic '1'. When the input = '1', the associated NMOS transistor is ON and the PMOS transistor is OFF. The output voltage is 0 volts (GND). One of the transistors is always OFF when the gate is in either of these logic states. Ideally, no current flows through the OFF transistor so the power dissipation is zero when the circuit is quiescent. i.e., when no transistors are switching [4]. Zero quiescent power dissipation is a principle advantage of CMOS over competing, transistor technologies. However, secondary effects are including sub threshold conduction, tunneling, and leakage lead to small amounts of static current flowing through the OFF transistor. Assuming the leakage current is constant so instantaneous and average power are the same; the static power dissipation is the product of total leakage current and the supply voltage [3].

In the next sub heading of static power we will discuss about the sub threshold conduction when transistors are off and leakage current through reverse-biased diodes.

3.1.1. Sub threshold Conduction when the Transistors are off

Both NMOS and PMOS transistors have a gate-source threshold voltage, below which the current (called threshold current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (V_{dd} might have been 5V and V_{th} for both NMOS and PMOS might have been 700mV). A special type of CMOS transistor with near zero threshold voltage is the naive transistor.

3.1.2. Leakage Current through Reverse-biased Diodes

Small reverse leakage currents are formed due to formations of reverse bias between diffusion regions and wells (for e.g., p-type diffusion vs. n-well), wells and substrate (for e.g., n-well vs. p-substrate). In modern process diode leakage is very small compared to sub threshold and tunneling current, so these may be neglected during power calculations [5].

3.2. Dynamic Power Dissipation

The primary dynamic dissipation component is charging the load capacitance. Suppose a load C is switched between GND and V_{DD} at an average frequency of f_{sw} .

Over any given interval of time T , the load will be charged and discharged $T_{f_{sw}}$ times. Current flows from the load to GND during discharge. In one complete charge/discharge cycle, a total charge of $Q=CV_{DD}$ is thus transferred from V_{DD} to GND[6].

The average dynamic power dissipation is

$$P_{dynamic} = \frac{1}{T} \int_0^T i_{DD}(t)V_{DD}dt = \frac{V_{DD}}{T} \int_0^T i_{DD}(t)dt$$

Taking the integral of the current over some interval T as the charge delivered during that time, we simply to

$$P_{dynamic} = \frac{V_{DD}}{T} [tf_{sw}CV_{DD}] = CV_{DD}^2f_{sw}$$

Because most gates do not switch every clock cycle, it is often more convenient to express switching frequency f_{sw} as an activity factor α times the clock frequency f . Now the power dynamic dissipation may be written as:

$$P_{dynamic} = \alpha CV_{DD}^2f$$

3.2.1. Charging and Discharging of Load Capacitances

CMOS circuits dissipates power by charging the various load capacitances (mostly gate and wire capacitances, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from the charged logic, current flows from the charged load capacitance (CL) to ground during discharge. Therefore, in a complete charge/discharge cycle, a total of $Q=CLV_{DD}$ is thus transferred from VDD to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by the average voltage again to get the characteristic switching power dissipated by a CMOS device= $0.5CV^2f$.

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor α , called the activity factor. Now, the dynamic power dissipation may be re-written as $P=\alpha CV^2f$. A clock in a system has an activity factor $\alpha=1$, since it rises and falls every cycle. Most data has an activity factor as 0.1. If correct load capacitance is estimated on a node together with its activity factor, the dynamic power dissipation at that node can be calculated effectively.

3.2.2. Short-circuit Power Dissipation

Since there is a finite rise/fall time for both PMOS and NMOS, during transition, for example, from OFF to ON, both the transistor will be on for a small period of time in which current will find a path directly from V_{DD} to ground, hence creating a short-circuit current. Short-circuit power dissipation increases with rise and fall time of the transistors [7].

To speed up designs, manufacturers have switched to constructions that have lower voltage thresholds but

because of this a modern NMOS transistor with a V_{th} of 200mV has a significant sub threshold leakage current. Designs (e.g. desktop processors) which include vast numbers of circuits which are not actively still consume power because of this leakage current. Leakage power is a significant portion of the total power consumed by such designs.

Multi-threshold CMOS (MTCMOS), now available from foundries, is one approach to managing leakage power. With MTCMOS, high V_{th} transistors are used in speed sensitive paths. Further technology advances that use even thinner gates dielectrics have an additional leakage component because of current tunneling through the extremely thin gate dielectric. Using high-k dielectrics instead of silicon dioxide that is the conventional gate dielectric allows similar device performance, but with a thicker gate insulator, thus avoiding this current. Leakage power reduction using new material and system designs is critical to sustainable scaling of CMOS [3,7]

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