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An Implementation 8×8 circuit of the 6T SRAM Bit cell by using Memory Array

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Abstract

Static Random access memory (SRAM) is useful building blocks area in many applications such as a data storage embedded applications, cache memories, microprocessors. Large SRAM arrays that are widely used as cache memory in microprocessors and application specific integrated circuits can occupy a significant portion of the die area. A Memory Array aggregates Flash memory components using a hot swappable form factor, and placing many of these modules into an array. The quest for larger data storage capacity lead the fabrication technology and memory development process to drive them to a more compact design rules.

Keyword: S-RAM, Circuit, Memory, Array, Bit, Cell, Line.

1. Introduction to Memory Array

A Memory Array aggregates Flash memory components using a hot swappable form factor, and placing many of these modules into an array designed from the ground up to take advantage of the capabilities of Flash. The result is that the SSD at least as they are used in legacy enterprise arrays, are similar to fibre channel conversion devices. We saw when fibre channel storage networks first came into being [1]. As the world became fibre only the need for such conversion devices no longer existed. The same may happen with SSD, as memory becomes increasingly the medium of choice much of the technology used today to retrofit it into the environment will no longer be needed.

2. Implementation 8×8 circuit of the 6T SRAM Bit cell

The quest for larger data storage capacity lead the fabrication technology and memory development process to drive them to a more compact design rules. The maximum realizable data storage capacity for a single chip semiconductor is approximately doubling every couple of years. Many VLSI circuits are using on chip memories for their subsystems, the capacity of single chip read/write memory commercially available today is 1GigaByte. But with the increasing memory size increases the number of transistors which in turn increases the power dissipation. Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds without dissipating too much power [2]. Number of stored data bits per unit area is a key design issue which determine storage capacity and so, the memory cost per bit. The time required to store or retrieve the data in the memory array is called the memory access time. The access time determines the memory speed, which is an important performance criterion of the memory array. Memories are of two types dynamic and static.

In Dynamic random access memory a capacitor is used to store the information and a transistor to access it. The cell information is degraded because of the junction leakage current. So it cannot store the data and read or write has to be done periodically even when cell is not accessed. But in Static Random Access Memory a latch is used, so the cell data is stored until the power is turned on. Due to low cost and high density, dram is widely used for main memory in personal and mainframe computers. SRAM is mainly used for cache memory in microprocessors, main frames and engineering workstations. As the technology decreases the power consumption becomes an important factor due to high transistor density, increased leakage currents and increase in interconnect parasitic. The power usage can be decreased by means of implementing appropriate methods. In first, we have discussed about the traditional 6T SRAM cell architecture which consists of hierarchical bitlines. Then the proposed architecture is discussed which is designed by replacing the hierarchical bitlines with twisted bitlines and the linear sense amplifier with the latch based sense amplifier. We designed a column select instead of column decoder and multiplexer which does the operation of both [3]. Twisted bitlines is being used for long time, but research shows that nobody has combined these techniques together to build a power

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efficient circuit. Column Select gives extra edge for our design to make the design more power efficient.

The hierarchical bitlines random access memory is shown in Fig 1. The architecture shown is an asynchronous design and is called Random access architecture because the memory location or addresses can be accessed randomly for reading or writing using the row or column decoder. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along which data flow into and out of cells, are called bitlines. A cell is accessed for reading or writing by selecting its row and column.

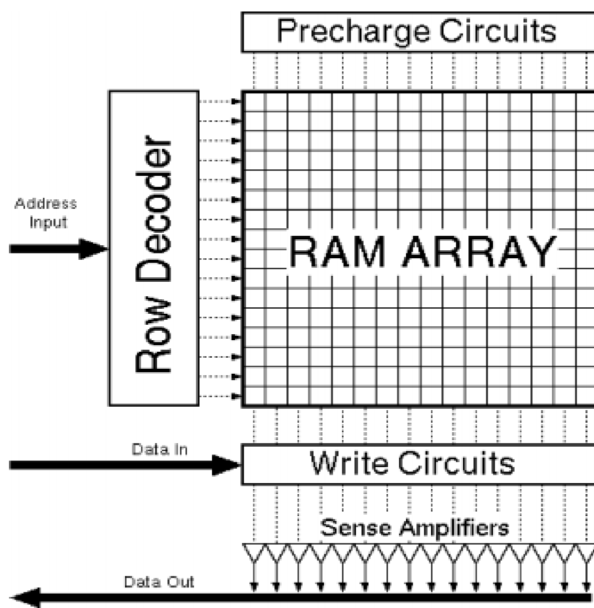

Figure 1: Traditional Architecture of SRAM Cell Array

Each cell is capable of storing 0 or 1. The row and column to be selected are determined by decoding information from the row and column decoders respectively.

3. Twisted Bit lines

In designing high performance circuits signal integrity is a critical factor. In the proposed architecture the parallel bit lines will introduce the cross coupling noise and in turn dissipates more power. This is the reason we used twisted bitlines to avoid the cross coupling effect. Twisting can be defined as the local reordering of parallel running interconnects lines [4]. It can be used for the bit line and/or word line schemes of memories or for busses in general. The twisted bit line format for 4 bitlines is shown in Fig 2.

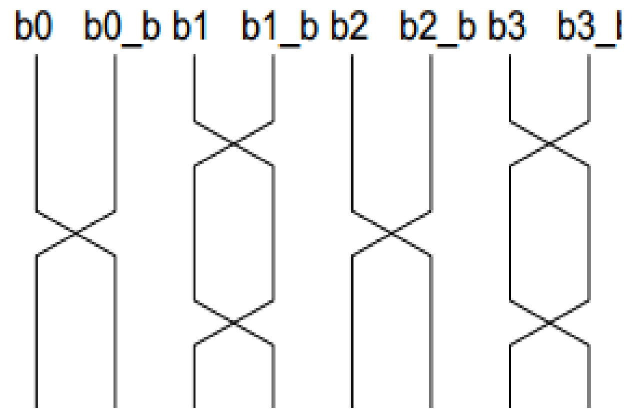

Figure 2: Twisted Bit line Architecture

4. Latched-based Sense Amplifier

The sense amplifiers need to amplify the data which is present on the bitlines during the read operation. The memory cells are weak due to their small size, and hence cannot the discharge the bitlines fast enough. Also, the bitlines continue to slew till a large differential voltage is formed between them [5]. This causes significant power dissipation since the bitlines have large capacitances. Hence, by limiting the word line pulse width we can control the amount of charge pulled down by the bitlines and hence limit power dissipation. The latched-based architecture is shown in the Fig. 3.

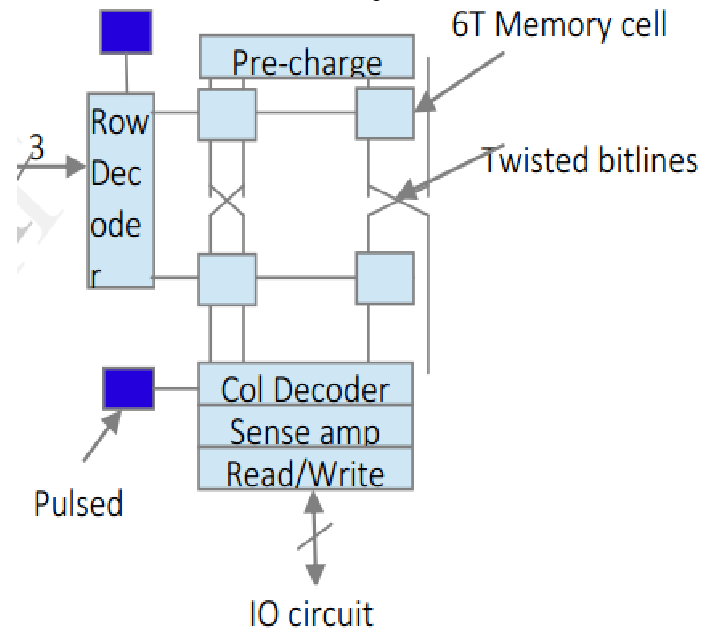

Figure 3: Lateched-based Architecture

The electrical representation of the architecture was also created for the clearer estimation of its working. The electrical representation is shown in Fig. 4.

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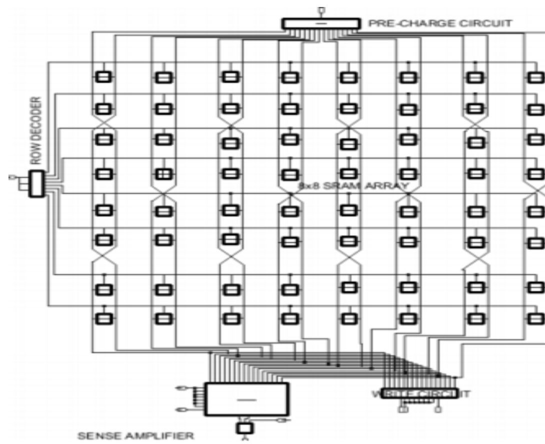

Figure 4: Schematic of Proposed Architecture in electric

The schematic circuit of 8×8 circuit is shown in Fig. 5.

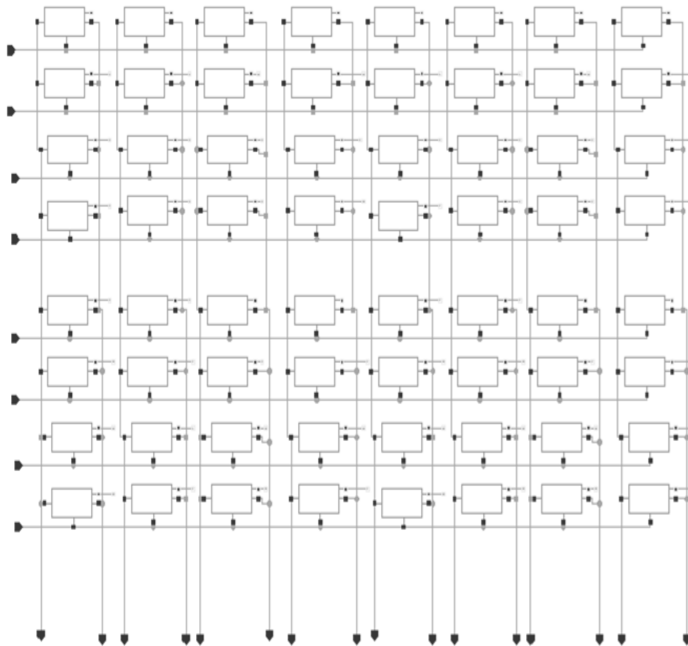

Figure 5: Schematic diagram of 8×8

5. Memory Read and Write '1' and '0'

To the operation first we select all the column decoder's inputs to '1' and row decoder inputs to '0'.Then the phi signal is activated which is used to precharge the bit and bit_b to the required voltage levels. When the Vwe is enabled the value of '1' is stored into the designated cell of the SRAM. Then to perform the read operation we enable Vsae i.e. the sense amplifier signal which is used to read '1' which we have written when Vwe is enabled. From the simulation results we can see that the voltage is 1.10v which is approximately 1v. Hence, the read and write operation is performed accurately for '1'. The Read and Write operation output for '1' is shown in Fig. 6.

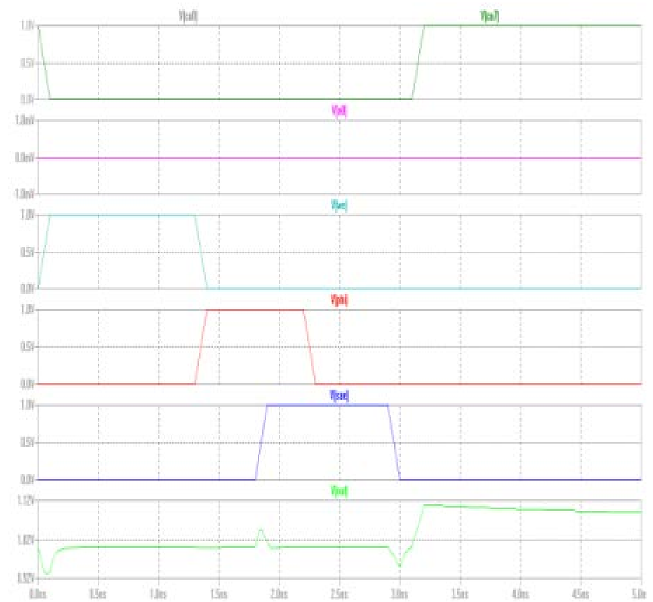

Figure 6: Output for Read and Write operation for 1

Then the same process is followed for the Read and Write operation '0' in Fig.7.

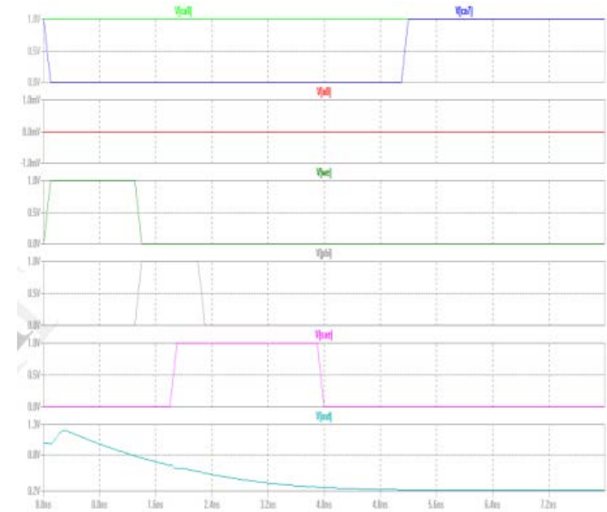

Figure 7: Read and Write Operation for '0'

6. Signal to noise Margin

Static noise margin (SNM) is an important parameter of SRAM cell. Static noise margin is defined as the maximum amplitude of circuit's direct current noise which the storage unit can endure with, and it is the measure of storage unit's ability against interference [6]. If the current noise exceeds the max amplitude, error flipping will occur at the storage nodes of the cell. With the development of integrated circuit, supply voltage becomes lower, and the external noise becomes relatively larger. Static noise margin will be decreased with the low supply voltage. Static Noise Margin

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determines and checks whether the cell is written '0' or '1'. The SNM is estimated 0.4V when compared to 0.6V. The low the value of SNM SRAM cell is more stable.

7. Conclusion

The analysis of the SRAMs has been done by designing the row and column decoder. With the help of those, the read and write data has been analyzed in the form of timing diagram for the required analysis of different SRAMs. For this its architecture along with the row and column decoder has been attempted. Further, the SRAM structures 8×8 bit SRAM have been explored.

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