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# A Review on Analysis of 4-bit Comparator using Different Full-Adder Logic Style with Different Technologies

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**Abstract:**
In era of electronics comparator is most important digital combinatorial circuit which compares two digital or analog signals, but outputs alway digital. With enhancement of technology optimization of digital circuit design improving day by day at the cost of complexity .In this review paper some thoughts on performance of different dynamic comparators is discussed. Many versions of dynamic comparator using different logic style of full-adders is proposed. The purpose is to find the high speed, low power and minimum area of dynamic comparator design. There are more than one technique to design CMOS comparators. By using different logic styles of comparators it is used accordance with application in specific need. The comparative analysis of 4-bit comparator architecture using different technologies. The simulation would be done on TANNER EDA using different VLSI technologies CMOS, CPL, DPL, DVL, GDI, TG, CNTFET, GDI and TG. The GDI and TG technologies allow to use less transistor count and power consumption and delay as compare to CMOS logic and lowers the term transistor count as compared to CMOS,CPL and DPL.

**Keywords:** 4-bit Comparator design, CMOS (Complementary Metal Oxide Semiconductor), GDI (Gate Diffusion Input), TG (Transmission Gate), Low Power Dissipation, Delay.

## 1. INTRODUCTION

Now a days the electronics world intended to round off zero dynamic power dissipation and delay of the digital combinatorial circuit , area minimization is too major constraint of comparator circuit design using adders. With the advancement of technologies by decreasing transistor count area is minimized. Full adder is heart of any digital processor and here implementation of various types of technology based 4-bit comparator design using basic full-adder circuit. There are many sort of techniques compared on the basis of transistor count, delay and power dissipation of 4-bit comparator architecture.

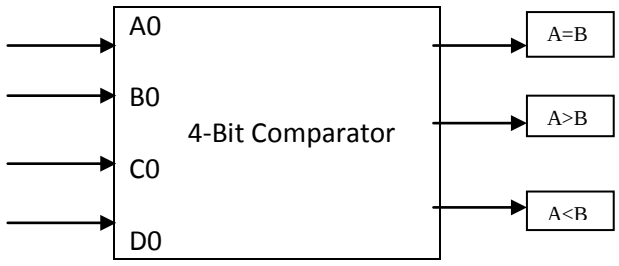


**Figure 1. 4-Bit Comparator**

**1.1CMOS (Complementary Metal Oxide Semiconductor)**: CMOS circuit is combination of two transistors PMOS and NMOS that's why the word complementary introduced because actions of one Transistor used in CMOS cell complement of one and other. Transistor count in CMOS,GDI and in TG is quiet low as compared to DPL or DVL technology, But in GDI and TG has much less transistor count as compared to both DPL and DVL module based technologies.

**1.2CPL (Complementary Pass Transistor Logic):** CPL has complementary inputs/outputs using NMOS transistors and CMOS output inverters. It features small stack height and internal node low swing, which lowers the power consumption. CPL's limitation creates dominating static power consumption because of low swing at the gates of inverters.

**1.3DPL (Double Pass-Transistor Logic):** DPL too uses complementary transistors to yields full swing operation and lowers dc power consumption. This eliminates the need for restoration circuitry. One disadvantage of DPL is that has large area due to PMOS transistors.

**1.4 DVL (Double Valued Logic):** Features of both CPL and DPL are recognized in DVL to minimize the transistor count which in turn decreases the area and input loads.

**1.5 TG (Transmission Gate):** Transmission gate is pass transistor logic with complementary use of transistor to construct TG gates to realize logic functions using small number of complementary transistors. It solves the



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problem of low logic level swing by using PMOS and NMOS transistor implementation. There is no universal library for PTL-logic based design.

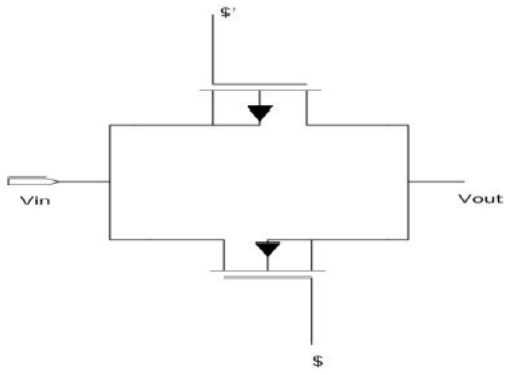


**Figure 2: Basic Transmission Gate**

A different low-power design for digital combinatorial circuits allows overcome limitations of above mentioned problems that Gate Diffusion Input which is efficient method to optimize area and delay as well as discussed below:

**1.6 GDI (Gate Diffusion Input):** Basic cell is exact explanation of CMOS inverter having three inputs (P, N and G) as shown in figure:

1. P (Input to source/drain of PMOS).
2. N (Input to source/drain of NMOS).
3. G (Common Input to gates of PMOS and NMOS).

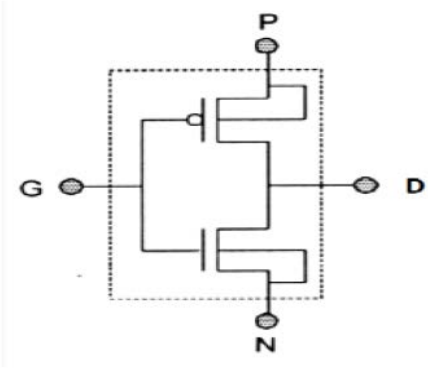


**Figure 3: Basic GDI cell.**

**2. Performance Parameters**

GDI overcomes the several limitations of the PTL-based design of complexity, switching activity, power dissipation, and speed and area optimization.

**2.1 Supply Voltage Noise-Error:** In order to assess the effects of noise sources due to external influences such as radio frequency signals ,voltage drop on power lines or ground connections, unterminated, signal lines and lines with non-uniform impedance characteristics.

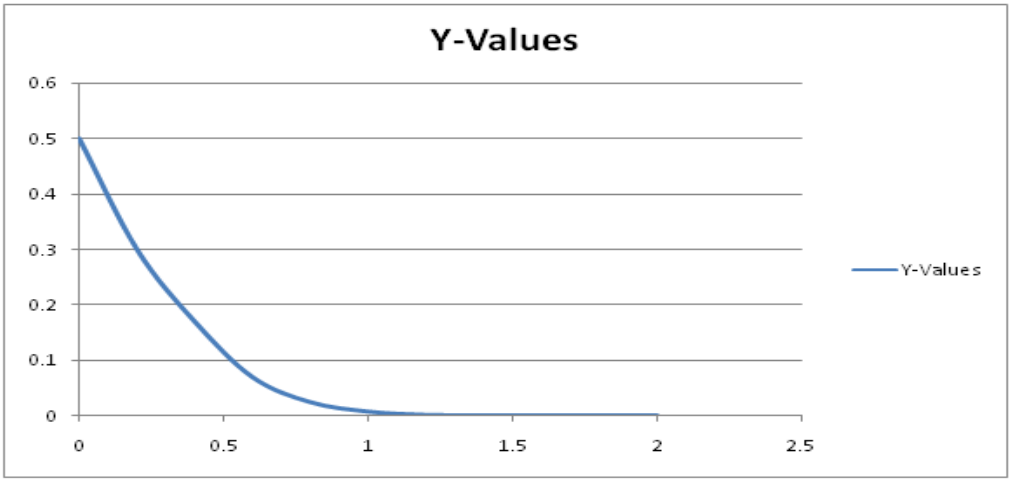


**Figure 4: Probability of error versus supply voltage.**

Major advantages of scaling devices due to which smaller gate delay time that is higher operating frequencies and lower power dissipation, delay and area of the circuit. Noise inputs are due to mutual inductive and capacitive coupling and these alone could impose practical limitations on the lowest usable operating voltages.

**2.2 Dynamic power dissipation**

In all CMOS technologies, dynamic power dissipation is main issue of concern.

$Pd = CL.(Vdd).2.a.f$ (2.1)

Where CL is load capacitance, Vdd is supply voltage is switching activity and f is frequency.

**2.3 Delay in CMOS and PTL circuits:** Delay is not function of circuit technology and circuit architecture, depends on wire length and width.



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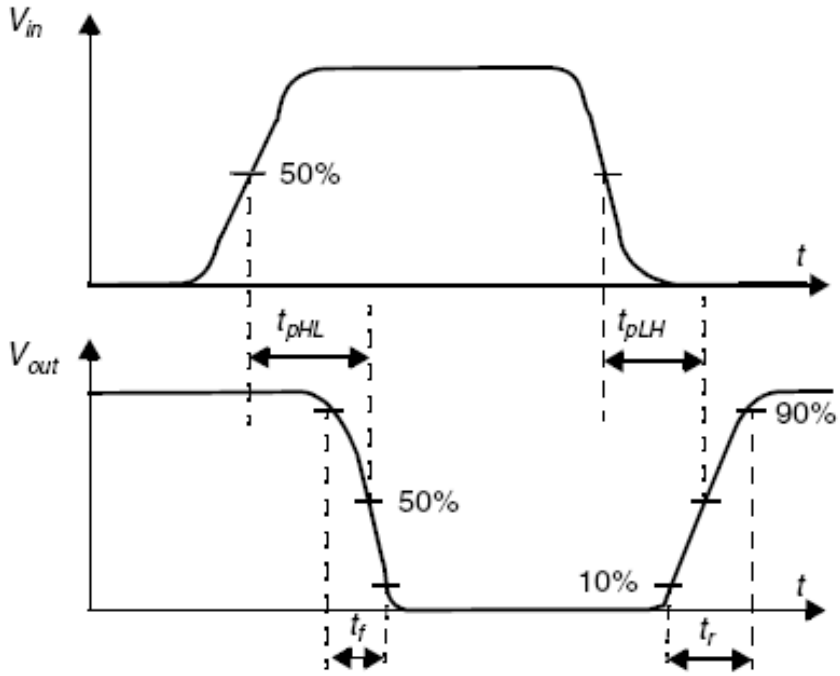


**Figure 5:**

The tpHL defines the gate response time when low to high transition while tpLH refers to a high to low (or negative) transition. Total propagation delay (£) from figure.6

£= (tpHL+tpLH)/2 (2.2)

Delay is directly proportional to square of wire-length and as wire-width increases.

**3. Literature Survey**

**[1]. Eric R. Menendez et.al,** In this paper two designs for CMOS comparators one for high speed and low power applications. Hierarchical pipelined comparators which can be optimized for delay, area or power consumption. To enable a fair comparison with previously reported approaches design simulated on AMIS 5V 0.5um and on SPICE 1.2V 100nm process and 37% speed improvement with latency of 1.33ns.High speed design accommodate percharge time to compute intermediate signals that speeds up 64-bit circuit design.

**[2]. Arkadiy Morgenstern et. al,** this paper depicts a new low power combinatorial circuit design which allows reducing power consumption, propagation delay and area of that circuit with low complexity. Performance realizations of CMOS (Complementary Metal Oxide Semiconductor) and PTL (Pass Transistor Logic) techniques.

**[3]. Laxmi Kumare et. al,** this paper presents a proposed design of different digital circuits whose power can be reduced by 40% - 60% using appropriate circuitry. Gate diffusion input is based on Shannon expansion for lower power dissipation. For ripple adder GDI saves 53.3%, 55.6% d, 75.6% power and reduces delay 25.4%, 3.4%, 9.6% for CLA adder, Bit magnitude comparator and ripple adder. All circuits are simulated on VIRTUOSO SPECTRE at 180nm technology in CADENCE. Analysis concludes that GDI is power efficient and high speed combinatorial logic.

**[4]. Chandrahash Patel et.al,** in this paper designing is done with the help of Full adder which is heart of any digital processor. The analysis and comparison of different logic styles of comparator using various logic style of full-adder. Its advantage of less area and routing wires numbers decremented compare to other showed in paper. So it depends on the designer and its requirement which logic style is to be used and can be useful for implementation of higher order design.

**[5].Vandana Choudary et.al, this** paper presents a new design of comparator with the help of full adder which are the basic building blocks of ALU. Main aim of the technologies to decrease transistor count to have more devices on a single chip layout. Hybrid comparator logic style provides low power and low area. By using this architecture

**[6]. Vipin V. Kashti et.al,** this paper presents a efficient, low power, fast response Carbon Nano Tube Field Effect Transistor based comparator which have better



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performance as compared to CMOS devices. Both CMOS and CNTFET comparators are simulated in CADENCE. The performance of parameters such as delay, power dissipation, speed is much more efficient in contrast to CMOS comparator. The future work effort to make it adaptable for higher comparator configuaration.

**4. Conclusions and Future work**

In this review paper, major component of ADC that speeds-it-up and enhanced its battery life is comparator. In our work various improved comparator circuits are studied with the view to reduce area to make it adaptable for high speed using GDI and TG technology .The 4-bit comparator is realized by using different logic style adder cells abutting NOR and AND cells on an alternate 180nm , 130nm technology. At different supply voltages performance of various adder design styles are checked thus dynamic power dissipation quadraticaly effected, power decreased without requiring any special technologies. To achieve low power, less transistor count GDI and TG technology based 4-bit comparator is designed. For optimization of power and delay best option to use 9T-full adder or SERF full adder to design comparator Due to the promising feature of carbon-based devices the possibility of replacing silicon device with carbon devices cannot be neglected. However recent research has shown that Carbon-Nano-Tube has a great potential in circuit designing not only reduces power consumption, but also increase speed substantially. Using adder logic with less transistor count will be our future consideration using CNTFET technology based higher order comparator design.

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