ISSN: 2348 - 2117

International Journal of Engineering Technology and Computer Research (IJETCR)
Available Online at www.ijetcr.org
Volume 3; Issue 2; Page No. 169-171

# Design and Analysis of Storage Element using different Technologies

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**ABSTRACT**

Over the past decade, Power consumption of digital systems has been continuously increasing. The need of low power design is becoming a vital parameter in high performance digital systems. This paper enumerates low power , high speed designs of D flip flop. It presents various techniques to minimize the power consumption of the digital circuits. In this paper implementation of D flip flop using CMOS TG(Transmission gates) Technique, GDI(Gate diffusion input ) Technique is presented and compared. The design and simulation is done using Tanner EDA and 180nm technology. In this the proposed designs are best energy efficient and having an efficient improvement in Transistor count and power consumption.

**Key Words:** Low power, less transistors, D flips flop, TG, GDI

## INTRODUCTION

The latest advancement in computing technology has set a goal of high performance with low power consumption for VLSI designer. Technology scaling of transistor feature size has provided a remarkable innovation in silicon industry for the last three decades. Designers are striving for small silicon Area, higher speeds, low power consumption and reliability due to ever increasing demand of portable electronics. Hence the power optimization techniques should be applied at different levels of the digital design. One of these techniques is to use low power logic styles which should be used in design of flip flops. A flip flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can either a flip flop in a variety of ways and gives rise to different types of flip flops. Among all the types of flip flops, mostly D flip flop are used. They are transparent during the entire time when the clock signal is asserted. There are situations when it is more useful to have the output change only at the rising edge or the falling edge of the clock signal, which is usually the controlling clock signal. In this paper different type of D flip flop architectures are implemented and compared using Tanner EDA and 180nm technology. They are CMOS transmission gates and GDI technology. All these flip flops are aiming at reduction of power, delay and area.

### Implementation of D flip flop

DFF implementation will done using Tanner EDA and using 180nm technology.

### *A. CMOS D flip flop Implementation using TG(Transmission Gates)*

In this the D FF is designed using CMOS transmission gates in master slave configuration. In this the master section is driven by the clock signal and the slave section is driven by inverted clock signal. The common circuit symbol for a transmission gate depicts the bidirectional nature of the circuit, the common circuit symbol of TG and schematic of TG is shown in figure1& 2.

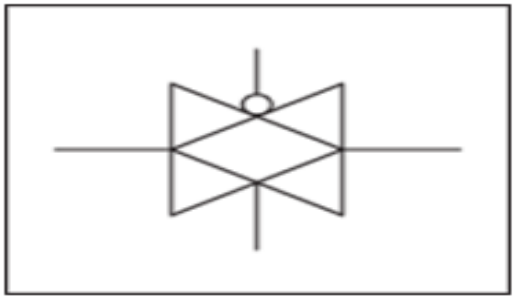

**Figure 1: Circuit symbol**

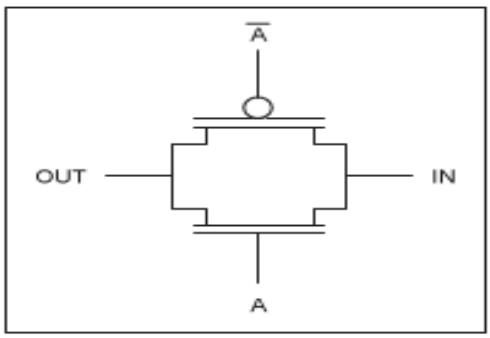


**Figure 2: Schematic representation of transmission gate**



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Transmission gate and inverters utilized to implement D flip flop as illustrated in Figure.3

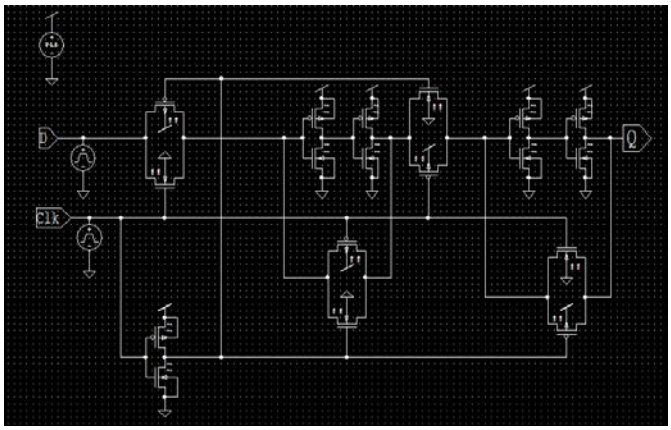


**Figure 3: CMOS D flip flop implementation using TG**

*Simulation waveform of CMOS DFF using TG as shown in figure. 4*

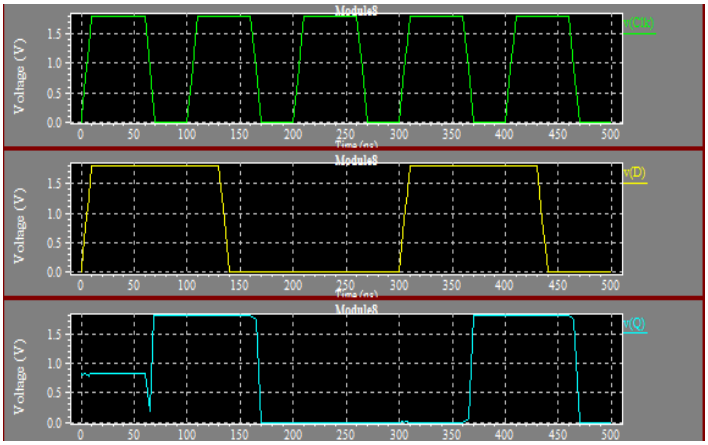


**Figure 4: waveform of CMOS DFF using TG**

The CMOS DFF using transmission gate technology is much efficient than others. The flip flop changes its state at the falling edge of the clock signal. Transmission gate is an important structure implemented using CMOS Integrated circuit that sustains switch function, efficient layout and logic reduction.

### *A. D FF implementation using GDI Technology*

Gate diffusion technique is defined as a new technique of low power digital systems. Gdi technique can be used to design fast, low power circuits using only few transistors and reduced the power consumption.GDI technique is a new technique used of best power delay product. It stands foe Gate diffusion input because inputs are directly diffused into the gates of N type and P type Transistors. This technique is based on a simple cell, which has 3 inputs and 1 output. The basic GDI cell shown in figure.5

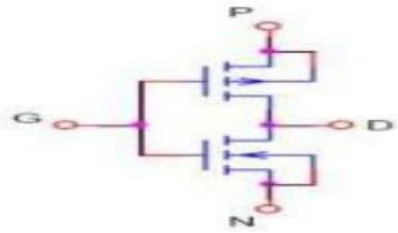


**Figure 5: Basic GDI cell**

Using GDI Technique implementation of DFF is as shown in Figure.6

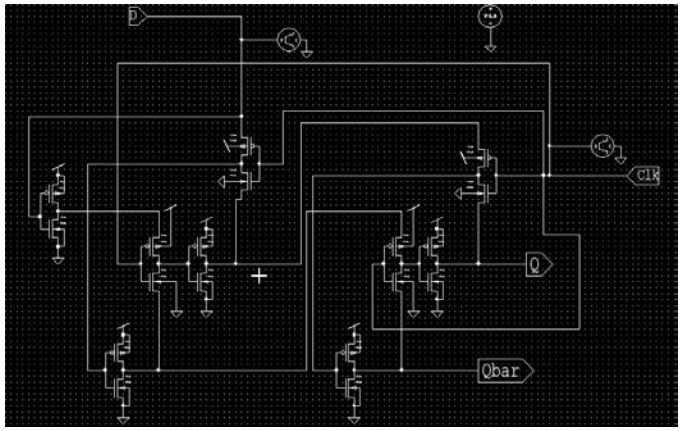


**Figure 6: DFF using Gate diffusion input technique**

In the GDI technique DFF is implemented using master slave configuration. The simulation waveform of GDI based D flip flop is shown in Figure.7

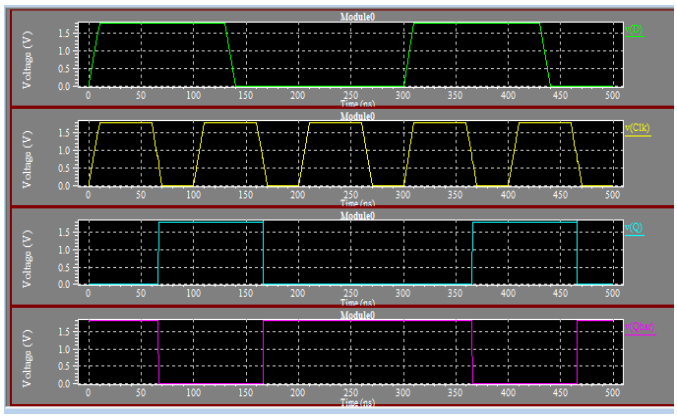


**Figure 7: waveform of GDI based DFF**

Implementation of D Flip flop is done using Tanner EDA and to design both TG based DFF and GDI based DFF 180nm technology used. In this length of PMOS is 0.18um and width of PMOS is 0.72um used, and length of NMOS is 0.18um and width of NMOS is 0.36 used for designing the D flip flop. By using both technologies TG and GDI the transistor count is less than other conventional methods. In these 18 transistors is used. Comparison of TG and GDI is shown in Table no.1.In this comparison is done on the basis of transistor count, Average power and Delay as shown in table 1.

**Table.1 Comparison of TG &GDI based DFF**

| Technique | Length of PMOS | Width of PMOS | Length of NMOS | Width of NMOS | Transistor count | Average power(w) | Delay |
|---|---|---|---|---|---|---|---|
| TG | 0.18um | 0.72um | 0.18um | 0.36um | 18 | 3.587390e-005watts | 3.5589e-008 |
| GDI | 0.18um | 0.72um | 0.18um | 0.36um | 18 | 1.436226e-006 watts | 3.4831e-008 |

According to the simulation results, both technologies have less transistor count than other conventional methods. But in power delay product GDI is much better than TG and other methods. The simulation is done using Tanner EDA and 180nm technology and using 1.8v supply voltage.

**CONCLUSION:**

For low power applications DFF designed using TG and GDI technologies. Both have high speed and lower delay. In order to have lower power consumption we use GDI technique.GDI DFF is having less power consumption therefore its performance is best. In future work if some drawbacks Occurs in GDI Technique that will be overcome by using Modified GDI technique and Full Swing GDI technique.

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